1993

Design of an ultra low noise high bandwidth operational amplifier using complementary bipolar technology

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TITLE:

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DATE: May 30, 1993

DESIGN OF AN ULTRA LOW NOISE HIGH BANDWIDTH OPERATIONAL AMPLIFIER USING COMPLEMENTARY BIPOLAR TECHNOLOGY

by

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A Thesis

Presented to the Graduate Committee

of Lehigh University

in Candidacy for the Degree of

Master of Science

in

Electrical Engineering

May 1993

This thesis is accepted and approved in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering.

5/17/93

Date

Advisor in Charge

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ACKNOWLEDGMENTS

The definition and successful completion of this thesis would not have been possible without the support and encouragement of many key individuals. Primary guidance came from my advisor Dr. Douglas Frey. Great assistance was also rendered by my officemates at AT&T including Andrew Grochowski, Kenneth Gross, Ico Koullias, Frank Peters, John Rebar and Trudy Stetzler. I would also like to thank my supervisors at AT&T, namely Stephen Parks, William Ballamy and Paul Dorman. Their attention and support defined and sustained my efforts to pursue graduate studies.

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ABSTRACT

The design of an ultra low noise high bandwidth operational amplifier using a complimentary bipolar circuit technology is presented. Basic noise concepts are discussed and comparisons are made between voltage feedback and current feedback amplifier topologies with respect to noise performance. A hand analysis and computer simulations of a best case input stage circuit are performed. A voltage feedback operational amplifier circuit is presented along with qualitative and quantitative analyses as well as results from computer simulation. The amplifier achieves an input-referred noise voltage of less than 0.8 $nV/\sqrt{Hz}$, a gain bandwidth product of greater than 300 MHz and an open loop gain of 65 dB while still maintaining unity gain stability.

I. INTRODUCTION

The operational amplifier (op amp), introduced in the mid 1960's, has become one of the most widely used circuit elements in existence today. Used primarily in circuits employing the concept of negative feedback, the op amp provides designers great flexibility in designing gain and filtering elements. The op amp has a large open loop voltage gain which can be traded off for gain stability by the proper configuration of a minimal number of external components.

Because any real op amp can approach but not attain the characteristics of an ideal one, users must identify which particular characteristics are most important in being as close as possible to the ideal case. An ideal op amp is noiseless, has an infinite input impedance, zero input bias current, infinite open loop voltage gain, and zero output impedance. A non-ideal "real-life" op amp, whose equivalent circuit is shown in Figure 1, suffers from finite or non-zero valued characteristics.

The physical non-idealities of the devices and circuit architectures used to construct an integrated circuit op amp dictate several tradeoffs which must be considered in the design. It is the purpose of this paper to present the design process for an operational amplifier which displays low noise as one of its most important parameters. In addition to introducing the reader to the fundamentals of noise in electrical circuits, the design process will reveal specific tradeoffs involved in achieving low noise performance.

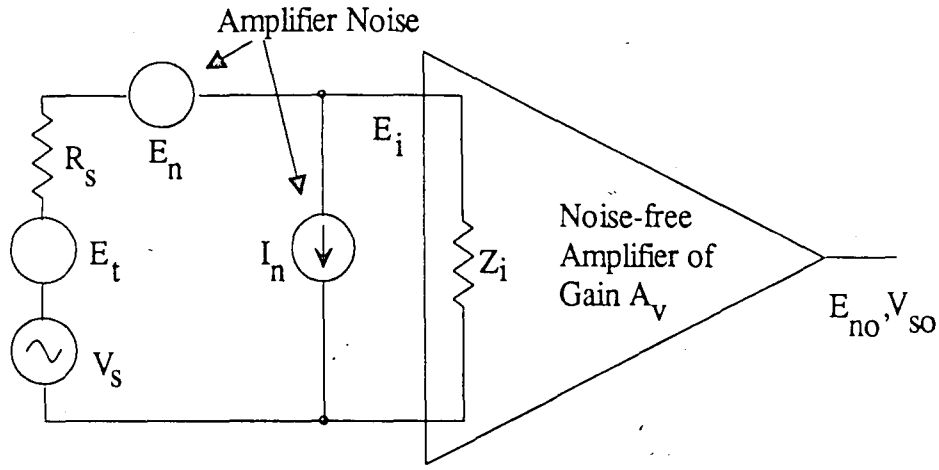


Figure 1. Non-Ideal Op Amp Model

With the noise performance of many sensors steadily improving, many applications can now demand amplifier noise performance on the order of $E_n \leq 1nV/\sqrt{Hz}$, where E_n represents an equivalent input-referred noise obtained by reflecting all system noise back to the input terminals. Many low noise op amps now on the market including the Linear Technology LT1028, Analog Devices AD797 and Comlinear CLC425 approach noise performance on that order, but each has limitations. Both the LT1028 and the AD797 become bandwidth limited above 100 MHz while the CLC425 cannot be used in applications requiring unity gain stability. The primary goal of the design presented in this paper is to overcome these limitations by offering unity gain stability up to a frequency of 300 MHz while maintaining a noise performance of $E_n \leq 1nV/\sqrt{Hz}$. Such an op amp would be useful in applications requiring precision instrumentation and low noise data acquisition.

An important step in the design process involves the selection of the basic operational amplifier topology to be used. A traditional approach is the voltage feedback amplifier, whose model is presented in Figure 2. It consists of a high input impedance

differential stage followed by at least one additional gain stage and then a low output impedance output stage. The output transfer characteristic is:

$$V_o = a(jf)V_D \tag{1.1}$$

where: $a(jf)$ = open loop voltage gain as a function of complex frequency

V_D = differential input voltage from (+) to (-) terminals

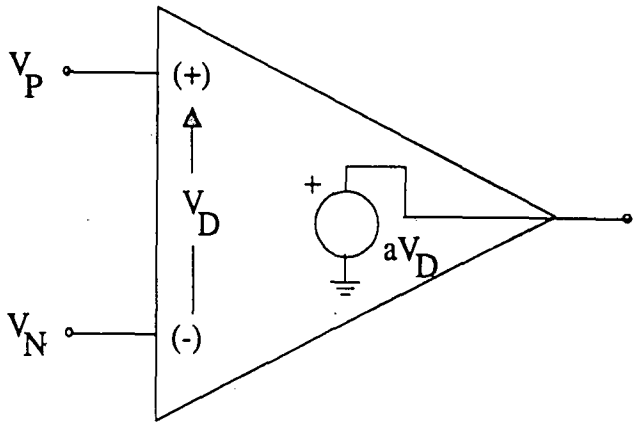


Figure 2. Voltage Feedback Op Amp Model

By connecting an external network as shown in Figure 3, a negative feedback path is formed which yields a closed loop transfer characteristic of the form:

$$A(jf) \triangleq \frac{V_o}{V_i} = \frac{1}{1 + 1/T(jf)} \tag{1.2}$$

where: $A(jf)$ = closed loop gain

and $T(jf)$ = loop gain which is given by:

$$T(jf) = \frac{a(jf)}{1 + R_2/R_1} \tag{1.3}$$

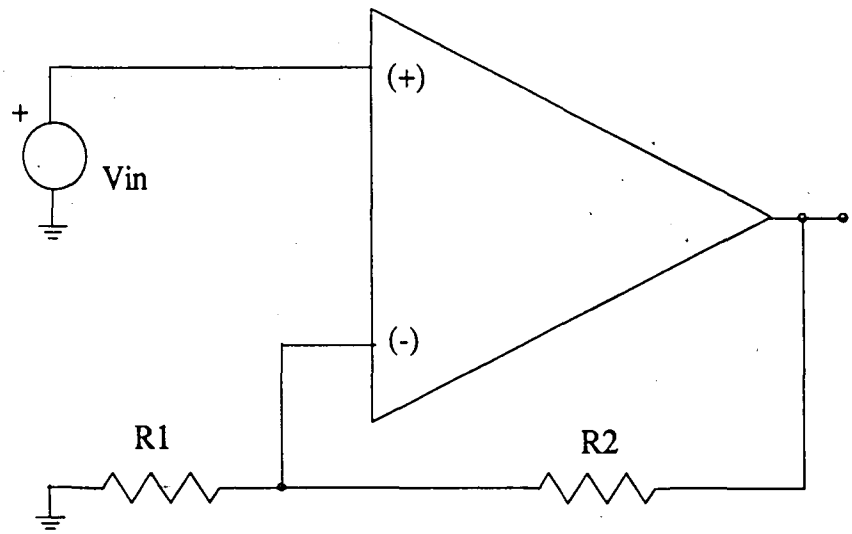


Figure 3. External Feedback Network

As represented by Figure 4, the closed loop gain of the circuit will remain constant as frequency is increased until a point f_A is reached at which the gain begins to roll off. This point defines the closed loop bandwidth of the voltage feedback amplifier.

Another approach to op amp design is the current feedback amplifier, shown in Figure 5. This architecture makes use of a unity gain input impedance buffer which, because of its low output impedance, allows current to easily flow in or out of the inverting input node of the amplifier. Signal processing is done almost entirely in the form of currents instead of voltages, with the exception of the output stage which consists of a transimpedance (current-to-voltage) amplifier. When external components

are connected in the same manner as was shown in Figure 3, the closed loop gain of the circuit is identical to Equation (1.2), but the loop gain now becomes:

$$T(jf) = \frac{z(jf)}{R_2} \tag{1.4}$$

where: $z(jf)$ = the transimpedance gain of the amplifier in Volts/Amp

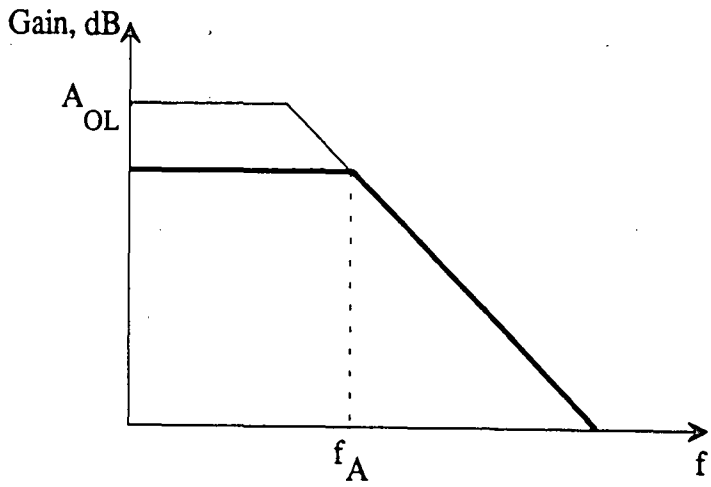


Figure 4. Closed Loop Gain Versus Frequency for a Voltage Feedback Op Amp

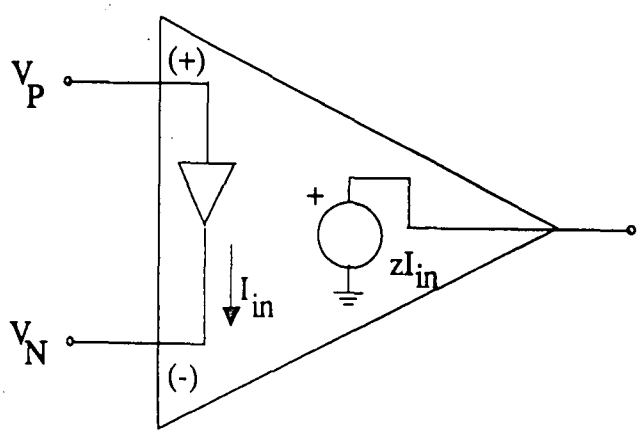


Figure 5. Current Feedback Op Amp Model

Now the loop gain of the circuit depends on R_2 alone. This means that the gain of the amplifier can be set independently of the roll-off point f_A, a great advantage for users desiring high gain at high frequencies. Currents can be switched faster than voltages because the effects of stray inductance are usually less severe than the effects of stray capacitance. The current feedback approach, because it processes currents instead of voltages, provides superior performance over the voltage feedback approach in many areas including speed and frequency response.

Unfortunately, low noise performance is one of the few areas in which current mode architectures lose out to voltage mode circuits. Low noise circuits benefit from input stages having high gain, a requirement which cannot be satisfied by the unity gain input buffer present in the current feedback design. This is a major reason why almost all commercial solutions for low noise operational amplifiers utilize a voltage feedback architecture, and why the voltage feedback approach was chosen for the design in this paper.

After presenting a brief overview of types of noise and how noise sources are modeled, a discussion of the physical sources of noise in a bipolar transistor will be presented. A hand analysis of a simple differential pair will lead to further analyses aimed at characterizing a best possible input stage in terms of noise performance. The design process for a voltage feedback operational amplifier will be presented along with computer simulation results.

II. A DISCUSSION ABOUT NOISE

Noise can be defined as any unwanted disturbance that obscures or interferes with a desired signal. The source of disturbance can be either external or internal to the circuit. External noise can often be reduced by proper shielding and grounding techniques, but little can be done by a user to suppress noise generated internally due to the inherent physical properties of semiconductor bulk regions and pn junctions. While the largest allowable input signal level of a circuit is set by its architecture, the smallest input signal and therefore the dynamic range of a circuit is determined by noise.

Noise can be described as a totally random signal in both amplitude and phase. The instantaneous value of a noise waveform measured over time often displays a Gaussian distribution as shown in Figure 6. The probability of an instantaneous voltage

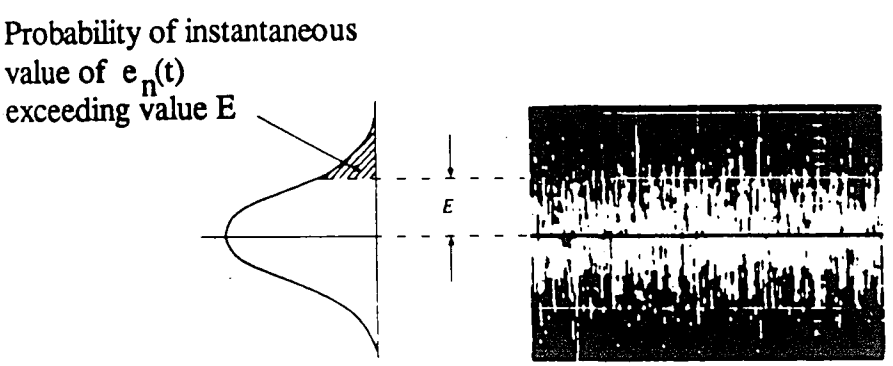


Figure 6. Gaussian Distribution Of Instantaneous Noise Waveform

or current value exceeding a value E is represented by the shaded area under the curve, given that the total area under the curve is unity. Measurements of noise are made by specifying the long term root-mean-square (RMS) value of a noise signal. Two independent noise sources having no relationship between their instantaneous voltage values are said to be "uncorrelated" and will add in an RMS fashion as shown in Figure 7.

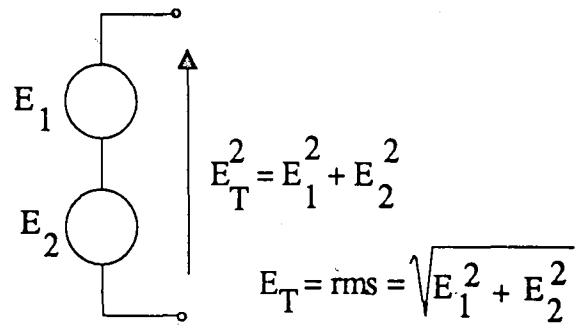


Figure 7. Root-Mean-Square Addition Of Uncorrelated Noise Sources

Different types of noise are classified according to the mechanisms which are believed to cause them. Three of the most commonly considered types are "thermal" noise, "shot" noise and "1/f" noise.

"Thermal" noise, sometimes called "Johnson" or "Nyquist" noise, is caused by the thermally-excited and random vibration of charge carriers in a conductor. The average current through a conductor by itself is zero, but current fluctuation does occur from one instant to the next due to the random motion of electrons in the conductor. The amount of noise or instantaneous change from moment to moment is however dependent on the temperature, resistance and measurement bandwidth of the system. The RMS noise voltage E_t of a resistance R is given by:

$$E_t = \sqrt{4kTR\Delta f} \qquad (2.1)$$

where: k =Boltzmann's constant = $1.38 \times 10^{-23} W \sec / K$

T =Temperature of the conductor in Kelvin

Δf =noise bandwidth of the measuring system in Hertz

The resistance R can be either a desired circuit element resistance or a parasitic resistance. It should be noted that "noise bandwidth" is defined differently than the more commonly used "3dB bandwidth." The 3dB bandwidth of a circuit is defined as the frequency span between half-power points, as shown in Figure 8. The noise bandwidth of a circuit is the frequency span of a rectangularly shaped power gain curve equal in area to the area of the actual power gain curve, as shown in Figure 9.

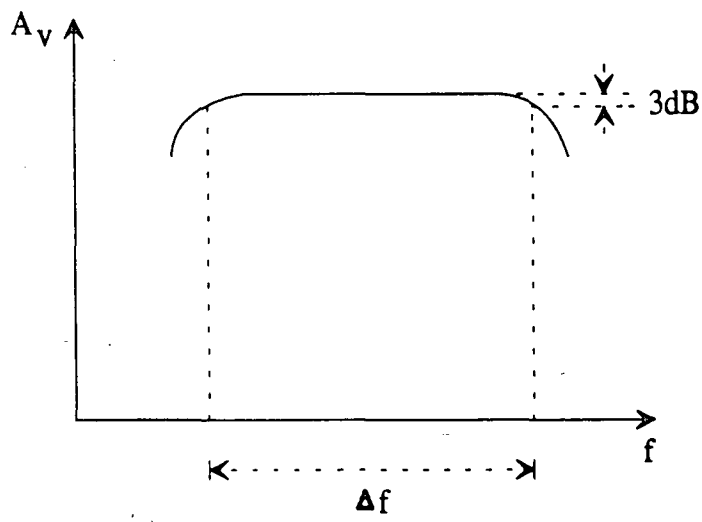


Figure 8. Definition of 3dB Bandwidth

For a given value of temperature and resistance, thermal noise is proportional to bandwidth and independent of frequency. Because a specific bandwidth of thermal noise

exhibits the same noise power content at high frequencies as it does at low frequencies, it is also referred to as "white" noise; just as the color white is made up of many colors, white noise is made up of many different frequency components.

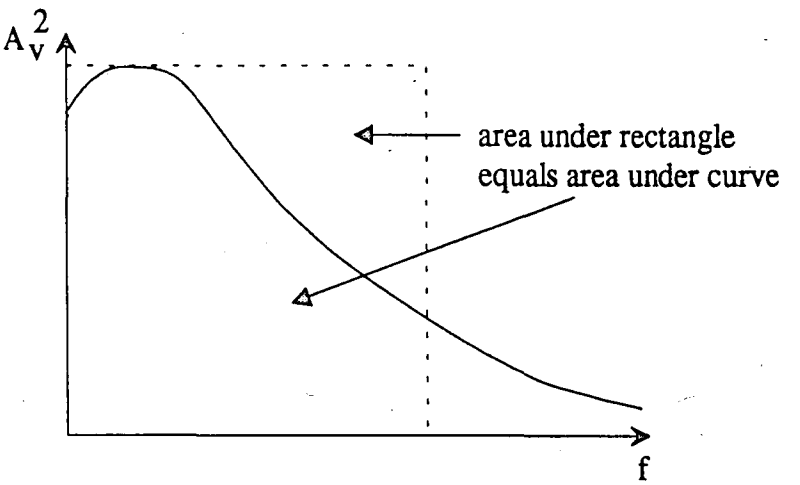


Figure 9. Definition of Noise Bandwidth

Thermal noise involves no **net** motion of carriers. Another type of noise called "shot" noise is associated with the non uniform motion of electrons in one direction in a pn junction. Current flow is really the sum of pulses of current caused by the flow of carriers, each one carrying a charge "q". The variation in these current pulses, seen as shot noise, produces a granular effect. Like thermal noise, shot noise is independent of frequency but dependent on bandwidth. The RMS value of a shot noise current is given by:

$$I_{sh} = \sqrt{2qI_{DC}\Delta f} \qquad (2.2)$$

where: q=electronic charge=$1.59 \times 10^{-19} C$

I_{DC}=direct current in Amperes

Δf =noise bandwidth of the measuring system in Hertz

The third type of noise most often considered, "1/f" or "flicker" noise, predominates at lower frequencies. Caused by the generation and recombination of carriers in surface energy states, 1/f noise gets its name from a noise power plot which follows the following characteristic:

$$P = \frac{1}{f^{\alpha}} \qquad (2.3)$$

where α falls between values of 0.8 and 1.3. This type of noise increases without limit as frequency decreases; frequencies of a few cycles per day exhibit 1/f noise. The noise power content for 1/f noise is equal for each decade of bandwidth. This means that the same level of noise power that exists in the range of frequencies from 1 to 10 Hertz will also exist in the range from 0.1 to 1 Hertz. Because the effects of 1/f noise decrease rapidly as frequency increases, contributions from this type of noise in high speed circuits like the one considered in this paper are negligible.

An understanding of different types of noise permits the visualization and synthesis of an equivalent model for a noisy amplifier. Further analysis of this model results in an expression for the equivalent input-referred noise of the amplifier. An investigation into the effects of noise on cascaded gain stages is then helpful in deciding how to approach the tradeoffs involved in designing an operational amplifier patterned after a classic multistage voltage feedback architecture.

Characterization of noise mechanisms allows a circuit designer to model their effects and develop a picture of how circuit architectures can be optimized for low noise.

Figure 1 presented a model for a non-ideal amplifier represented by an ideal "noise-free" amplifier with all voltage and current noise referred back to input sources E_n and I_n respectively. Voltage source E_t models the thermal noise contributed by the noiseless source resistance R_s. Noise sources E_n, I_n and E_t can be combined and modeled as a single noise source E_{ni} which is placed in series with V_s and R_s allowing further simplification of the model shown in Figure 1. Using simple voltage and current division principles, an expression for this equivalent input noise E_{ni} can be derived. If E_i represents the noise voltage at the input terminals of the noiseless amplifier having a gain of A_v, then the total noise at the output would be:

$$E_{no}^2 = A_v^2 E_i^2 \tag{2.4}$$

E_i^2 can be expressed as:

$$\left[\frac{(E_n^2 + E_t^2)Z_i^2}{(R_s + Z_i)^2} + \frac{I_n^2 Z_i^2 R_s^2}{(R_s + Z_i)^2}\right] \tag{2.5}$$

If the system gain from the input signal source V_s is called K_t, then:

$$K_t = \frac{V_o}{V_s} \tag{2.6}$$

Voltage division between R_s and Z_i yields the following expression for V_o:

$$V_o = \frac{A_v V_s Z_i}{R_s + Z_i} \tag{2.7}$$

Substitution of equation (2.7) into equation (2.6) yields the following expression for system gain:

$$K_t = \frac{A_v Z_i}{R_s + Z_i} \tag{2.8}$$

The total input noise E_{ni}^2 can now be expressed as:

$$E_{ni}^2 = \frac{E_{no}^2}{K_t^2} \tag{2.9}$$

The resultant expression for equivalent input noise E_{ni}^2 is:

$$E_{ni}^2 = E_t^2 + E_n^2 + I_n^2 R_s^2 \tag{2.10}$$

Using this result, all of a circuit's noise sources can be referred back to the input and then combined into a single equivalent noise source. The value of E_t can be calculated directly from equation (2.1), E_n can be found by setting the source resistance R_s to zero, and I_n can be found by using two different values of R_s and observing how the overall noise performance changes. Both parameters E_n and I_n must be specified to fully describe an amplifier's noise performance.

It should be noted that the noise performance demanded of an operational amplifier is largely dependent upon the noise content already present in the input signal. The amount of signal-to-noise degradation caused by the amplifier would ideally be as small as possible, but input signals already containing a sizable noise content may not benefit greatly from the use of an ultra-low noise amplifier.

The total noise of an amplifier can be minimized by locating and understanding the important noise sources in the structure. Figure 10 presents a cascaded network of noiseless two ports, each block contributing gain from its input port to its output port.

The total gain of the system is $G_{total} = G_1 G_2$. Equal values of noise of value $E_{injA} = E_{injB}$ are injected at point A and point B. The total output noise would be given by the following expression:

$$E_{total} = \left(E_{injA} G_1 + E_{injB}\right) G_2 \qquad (2.11)$$

or simplified as:

$$E_{total} = E_{injA} G_1 G_2 + E_{injB} G_2 \qquad (2.12)$$

Given the task of optimizing the network for low noise while maintaining a total gain of G_{total}, a designer would conclude that the total output noise consists mainly of first stage noise, provided that the gain G_1 is large. Since $G_{total} = G_1 G_2$ remains constant, attempts to increase G_2 while decreasing G_1 would be detrimental, so a sound approach would be

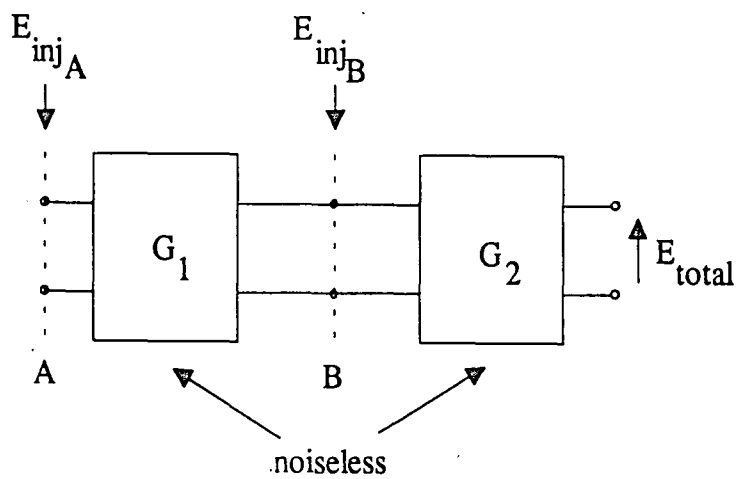


Figure 10. Noise Analysis of Cascaded Two Ports

to increase G_1. Similarly, greater benefit would result from attempts to decrease E_{injA} than to decrease E_{injB}. In summary, a low noise amplifier design benefits from an input stage with high gain and low front-end noise. This again was a major factor in the decision to pursue a voltage feedback architecture for the design presented in this paper.

One of the simplest models for a voltage feedback op amp is shown in Figure 11. It consists of a common-emitter differential input pair connected to a current mirror, a second gain stage, and a low output impedance unity gain output buffer. The transconductance (voltage-to-current) input stage provides gain and converts the input voltage to a signal current i_x. The second stage provides additional gain but, due to the compensation capacitance needed for loop stability, also limits the slew rate of the

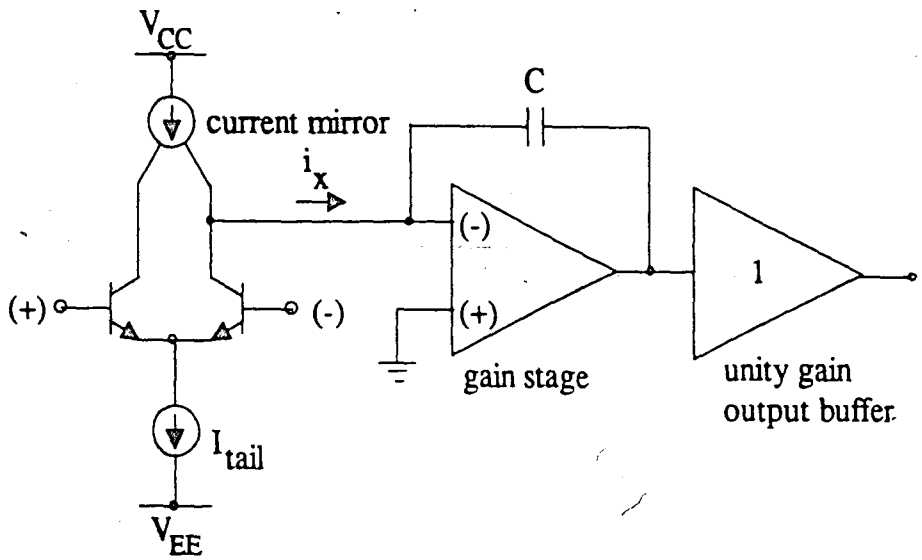


Figure 11. Voltage Feedback Op Amp Topology

amplifier. Finally, the output buffer provides current driving capability for the amplifier's load.

Successful low noise design demands that much attention be paid to minimizing the front-end noise present in the input stage. The use of a simple differential pair for the input stage requires an understanding first of noise in a single bipolar transistor and then of noise in a differential pair. Considering the simplified cross section of a vertical npn device shown in Figure 12, minority carriers can be visualized to diffuse and drift across

the base region, eventually reaching the base-collector depletion region where they are accelerated by the field existing there, finally reaching the collector. Because this process equates to a series of random current pulses arriving at the collector, the collector current I_C will exhibit shot noise as given by Equation (2.2). When referred back to the base, the effect of this shot noise will be diluted by the gain of the device. Base current, due to quantized carrier movement, also exhibits shot noise following the form of Equation (2.2).

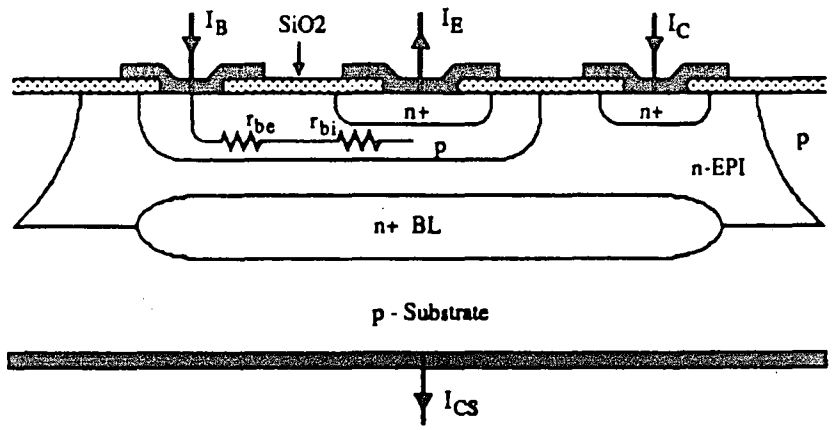


Figure 12. Cross Section of Vertical NPN Device

A non zero emitter resistance term exists in any real bipolar transistor. It consists of a fixed bulk emitter resistance r_E in series with a dynamic resistance term r_e. For those circuits with emitter degeneration resistors in series with the emitter, the resistance can simply be added to r_E for analysis purposes. To reduce thermal noise in the emitter, it is obvious that resistance should be minimized. Although external degeneration resistance can be omitted, the dynamic term r_e will always remain. For analysis purposes, the dynamic emitter resistance r_e of a bipolar transistor operating in the

forward active mode contributes a value of shot noise equal to the thermal noise voltage that would be contributed by an equivalent resistance of $r_e/2$. The dynamic emitter resistance r_e can be defined as follows:

$$r_e = \frac{kT}{qI_C} = \frac{1}{g_m} \tag{2.13}$$

where: k = Boltzmann's constant = $1.38 \cdot 10^{-23}\ W\,\mathrm{sec}/K$

T = Temperature in degrees Kelvin

q = Electronic charge = $1.6 \cdot 10^{-19}\ C$

I_C = Collector current in Amperes

g_m = Device transconductance in Siemens

Clearly, increasing the DC collector current of the device will decrease the resultant voltage noise due to the equivalent dynamic emitter resistance. This is a somewhat surprising and important realization. The reason for this relationship is that in the process of converting the noise current across the dynamic emitter resistance into a noise voltage, a factor of I_C contained in the current expression is multiplied by a factor of $1/I_C^2$ in the dynamic resistance expression, yielding a result that states that voltage noise reduction in a bipolar transistor actually occurs when DC collector current is increased.

As is the case with all engineering tradeoff situations, it is important to concentrate optimization efforts on those terms which contribute more significantly to the parameter in question. The minimization of base resistance is a primary concern with low noise design. As shown in Figure 12, the base resistance is made up of two

resistances in series, an extrinsic base resistance r_{bx} and an intrinsic base spreading resistance r_{bi}. Different texts will name these terms differently, but most follow the same basic concept. The values of both base resistance terms are dependent on the physical structure of the device which is dependent on technology constraints including parameters like linewidths and doping concentrations. The extrinsic base resistance can be minimized by decreasing the lateral distance between the emitter and base and by using multiple base contacts. The intrinsic base resistance is made small by laying out the emitter as a long stripe. Figure 13 shows the top view of a typical transistor constructed following these guidelines.

Considering the simple differential pair circuit shown in Figure 14, a best case analysis can be quickly performed to better understand the challenges of designing for an input-referred voltage noise of $1nV/\sqrt{Hz}$. Taking only the thermal noise contributions of the emitter and base regions into account, as well as the shot noise contributed by $r_e/2$, Equation (2.1) can be used to solve for R given that $E_t = 1nV/\sqrt{Hz}$ and $T = 298$ Kelvin for a bandwidth of $1Hz$. This amount of noise is produced by an equivalent resistance of 61 ohms. Following the proper low noise practice of omitting emitter degeneration resistance, this resistance would primarily consist of base and emitter resistance, as Figure 15 demonstrates. To meet the $1nV/\sqrt{Hz}$ goal, the following equality must be satisfied:

$$2(r_{bx} + r_{bi}) + 2r_E + r_e < 61 \text{ ohms} \qquad (2.14)$$

The emitter resistance r_E is usually quite small and can be neglected for this analysis. The dynamic emitter resistance r_e is dependent on the amount of tail current used to bias the differential pair. Using Equation (2.13) and a large dc current of 4 mA (equivalent

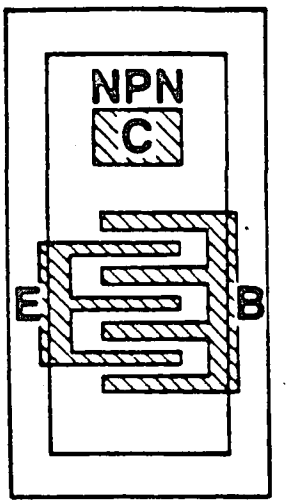


Figure 13. Top View Layout of Low Base Resistance Device

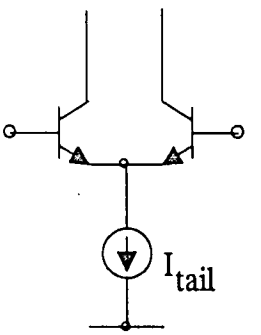


Figure 14. Input Stage Differential Pair

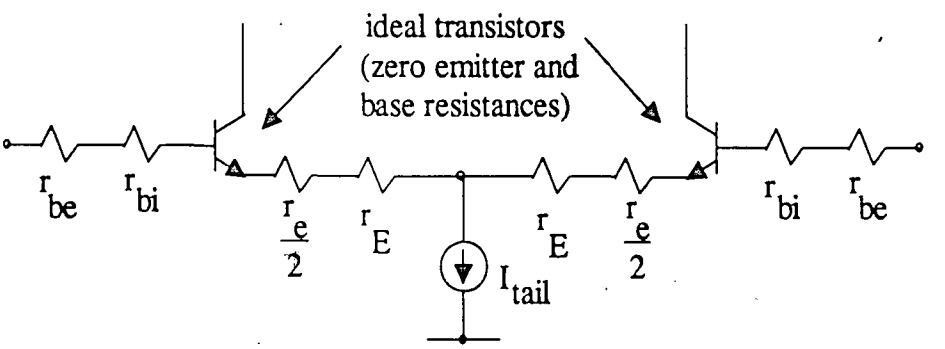


Figure 15. Modeling of Resistances In A Differential Pair

to an 8 mA tail current), r_e is calculated to be about 6.43 ohms. This leaves an allowable base resistance of:

$$(r_{bi} + r_{be}) = \frac{61 - 6.43}{2} = 27.29 \text{ ohms} \qquad (2.15)$$

Base resistances of this order push the current limits of high speed technologies. Considering that this analysis is best case and does not include noise contributions from the current source, load elements or any other circuit components, an input referred voltage noise of $1nV/\sqrt{Hz}$ is an aggressive goal.

III. THE DESIGN PROCESS

The primary design goal is the design of a unity gain stable voltage feedback operational amplifier having an input referred noise voltage no greater than $1nV/\sqrt{Hz}$ while maintaining a gain bandwidth product of at least 300 MHz. The process technology selected was AT&T's CBIC-V, a complementary bipolar process offering NPN and PNP f_t values of 11.2 GHz and 5.6 GHz, respectively. The design is performed assuming fabrication on a linear array, a pre-determined template of devices which are metallized with two layers of interconnect to complete processing. Although better characteristics can be achieved with a custom layout that reduces parasitics, the linear array offers a low cost alternative allowing designers to evaluate designs quickly and inexpensively. Appendix D describes CBIC-V in more detail.

Since the majority of a system's total noise is attributable to the front-end noise of the input stage, a logical first step in designing a low noise circuit would be to perform some initial simulations using a circuit like the one shown in Figure 16. The results obtained from such an analysis would establish a "best-case" baseline. The addition of additional circuit elements will certainly degrade noise performance, but not by an appreciable amount, assuming that front-end input stage noise is the major culprit.

A hand analysis of the input-referred voltage noise of the circuit shown in Figure 16 proceeds as follows. The 1 milliohm resistors R3 and R4 exist only to establish a DC bias point for the bases of transistors B1 and B2. Because of their low resistance value,

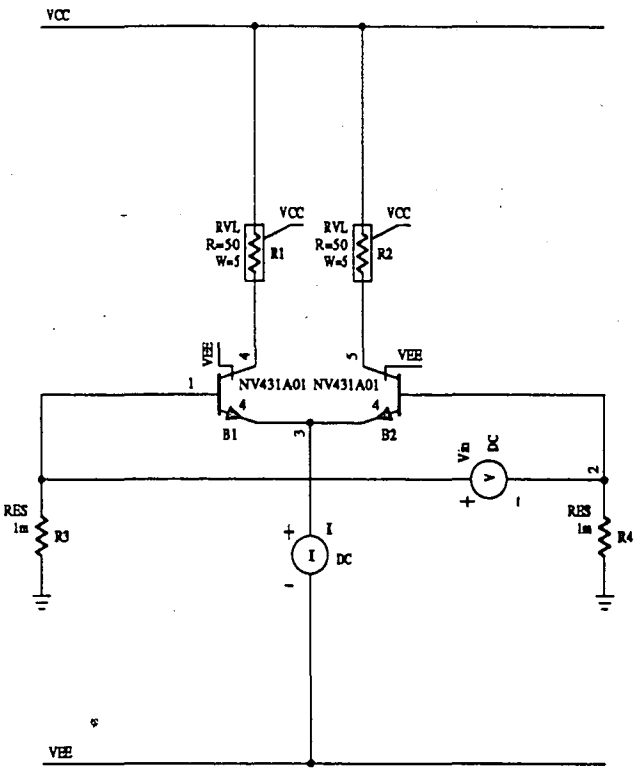


Figure 16. Input Stage For Best-Case Noise Analysis

they add negligible thermal noise. The input stage circuit shown consists of the emitter-coupled pair B1 and B2, each being a scaled NV431A01 device whose unscaled model parameters are shown in Appendix A. The total base resistance including both extrinsic and extrinsic components equals approximately 26.5 ohms for a single 12X device. B1 and B2 are both 48X devices as indicated by the scaling factor of 4 shown. This equates to four unscaled base resistances in parallel, or 26.5/4 = 6.625 ohms for the base resistance of each transistor. Assuming a tail current of 8 mA or 4 ma for each device,

the dynamic emitter resistance r_e is equal to 6.43 ohms as before. Using a value of 1 ohm for r_E, the total resistance in the input path of the differential pair is calculated:

$$\begin{aligned} &2(r_{be}+r_{bi})+2r_E+r_e \\ &=2(6.625)+2(1)+6.43=21.68ohms \end{aligned} \qquad (3.1)$$

From Equation (2.1), this resistance equates to an input-referred noise of 0.597 $nV/\sqrt{Hz}$ due to B1 and B2.

Resistors R1 and R2 also contribute to the total noise of the circuit, although not as significantly as the transistors do. Assuming R1 and R2 are of value R, each resistor contributes a noise voltage across itself of

$$E_{noise}=\sqrt{4kTR}\ nV/\sqrt{Hz} \qquad (3.2)$$

which translates to a current noise in the collector of

$$I_{noise}=\frac{E_n}{R}=\sqrt{\frac{4kT}{R}}\frac{nA}{\sqrt{Hz}} \qquad (3.3)$$

This current noise essentially appears in the emitter across r_e, therefore the input-referred noise due to R1 and R2, each having a resistance value of R, is equal to

$$E_{n,input}=\sqrt{\frac{4kT}{R}}\sqrt{2}(r_e) \qquad (3.4)$$

The factor of $\sqrt{2}$ occurs because the equal noise contributions of R1 and R2 add in an RMS fashion. For the 50 ohm resistors shown in Figure 16, Equation (3.4) works out to be $0.164nV/\sqrt{Hz}$. The total calculated input referred noise of the circuit including both B1 and B2 as well as R1 and R2 is

$$E_{n,total} = \sqrt{\left(E_{n,B1\&B2}{}^2 + E_{n,R1\&R2}{}^2\right)}$$
$$= \sqrt{\left(0.597^2 + 0.164^2\right)} = 0.619\,nV/\sqrt{Hz} \qquad (3.5)$$

An ADVICE simulation of the circuit, detailed in Appendix B, indicated an equivalent input noise of $0.616nV/\sqrt{Hz}$. This analysis indicates that with some proper design choices, a $1nV/\sqrt{Hz}$ input noise goal is quite achievable.

A complete schematic of the proposed circuit design is shown in Figure 17. It consists of an input stage, a second gain stage, a unity gain output buffer as well as biasing circuitry. The complementary bipolar process used consists of four terminal transistors, three terminal resistors and three terminal capacitors, the extra terminal in each case representing a connection to either the epitaxial layer (VCC) or the substrate (VEE). All simulations performed using the ADVICE simulator use device models which attempt to account for parasitics present in the actual physical structure of the IC. Before discussing AC performance, a discussion concerning the basic functioning of each part of the circuit and DC bias levels is in order.

Transistors B6, B7, B8 and B9 and resistors R4, R5, Rset, R14, R15, R16 and R17 set up a reference current of approximately 1 mA which gets mirrored by other devices to provide current sources for the entire circuit. The current flowing through Rset is calculated as follows:

$$I_{set} = \frac{(V_{CC} - V_{EE}) - V_{beB6} - V_{beB7} - V_{beB9} - V_{beB8}}{R4 + Rset + R5} \qquad (3.6)$$

Using a base-to-emitter voltage of 0.7V, supplies of +/-5 V and the values shown for the resistors, I_{set} is calculated to be exactly 1 mA. Resistors R14 and R17 act as bleed resistors which allow B6 and B8 enough current to operate in the forward active region. The collectors of B7 and B9 could be connected directly to VEE and VCC respectively if it were not for a problem of exceeding the collector-to-emitter breakdown voltage of 8 V. Resistors R15 and R16 allow enough voltage drop across themselves to correct the problem. Since the voltage at the emitter of B7 is approximately 4.1 V due to the 200 mV drop across R4 and the Vbe of B6, the voltage needed across R16 to keep B7 from breaking down is:

$$(4.1V - 8V) - V_{EE} = 1.1V \qquad (3.7)$$

given that VEE= -5 V. This means that for R16 equal to 20 Kohms, at least 55 uA must flow to develop a voltage drop of 1.1 V. A simulation of the DC operating point of the circuit confirms that more than 55 uA flows through R16 and therefore B7 is kept out of breakdown. A similar analysis can be performed for B9 and R15.

Transistors B5A, B5B, B8, B12, B17 and B18 and their associated emitter resistors each form a current source. Scaling of the 1 mA reference current can be calculated to a first order approximation to be equal to the ratio of the particular emitter resistance used in the current source to the emitter resistance R4 (for PNP sources) or to the emitter resistance R5 (for NPN sources). For example, the collector current flowing in B5A is roughly equal to:

$$I_{C,B5A} = I_{ref}\frac{R5}{R3A} = 1mA\frac{200\Omega}{50\Omega} = 4mA \qquad (3.8)$$

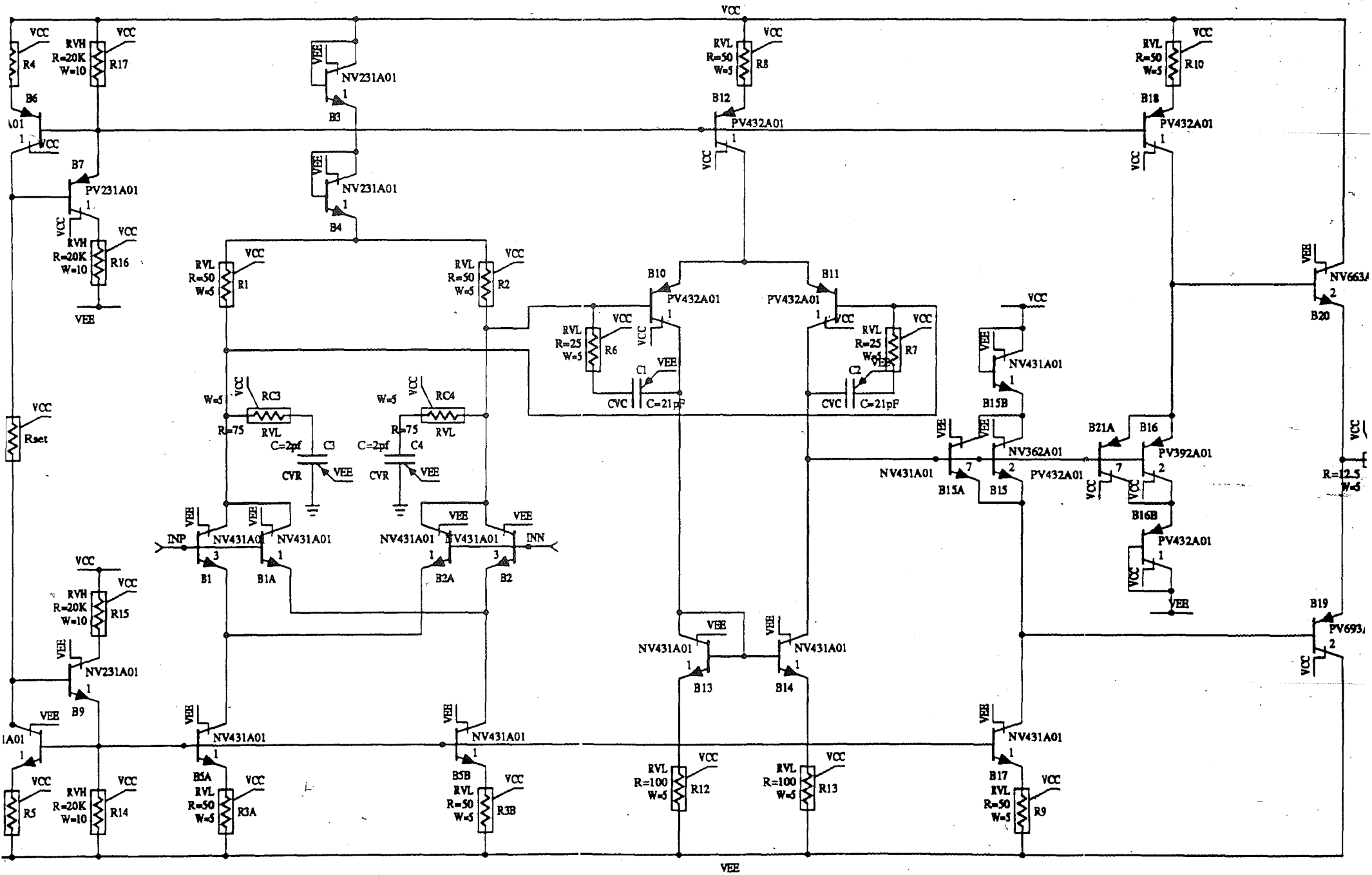


Figure 17. Schematic of Low Noise Op Amp

The current reference architecture used can be referred to as a simple current source with current gain. Transistors B7 and B9 improve current mirroring accuracy by making the current ratio mismatch dependent on a factor of $1/\beta_F^2$ rather than a factor of $1/\beta_F$ (which would be the case if B7 and B9 were not present and the collector-base junctions of B6 and B8 were shorted). Because of the finite small signal output resistance r_o associated with each current source transistor, changes in collector-to-emitter voltage will change the collector current slightly. This effect is more pronounced with PNP devices because of their lower Early voltage, V_A. The current reference and current source architecture used was found to provide adequate performance. Better temperature and processing variation stability could be obtained through the use of a bandgap reference circuit which is designed for positive tracking of absolute temperature (PTAT), although at the expense of additional supply current consumption.

The input stage shown in Figure 17 behaves very much like the previously discussed simple differential pair shown in Figure 16, with the exception of the emitter connections and tail current sources used. Figure 18 clarifies the modification made to the input stage, the purpose of which is to reduce the transconductance of the input stage in order to improve linearity, increase signal range and increase slew rate.

Transconductance reduction improves slew rate in the following manner. A traditional approach to amplifier design includes an input stage with a transconductance g_m followed by a frequency-compensated second gain stage. The slew rate of the circuit depends primarily on the size of capacitance used to compensate and the amount of current available from the input stage to charge the capacitance. It can be shown that the capacitance value is related to g_m and the unity gain frequency, and that when these

parameters are properly substituted into the equation for slew rate it becomes apparent that the slew rate of the amplifier is directly proportional to the charging current and the unity gain frequency and is inversely proportional to g_m. It then becomes an optimization exercise to reduce transconductance enough to improve the slew rate but not so much that input-referred noise is greatly affected.

The need to maintain a low noise input stage prohibits the more common practice of using emitter degeneration resistance in series with the emitters of the input devices, so the structure shown in Figure 18 is used to reduce transconductance without incurring the noise penalty of emitter resistors. Emitter degeneration typically works by feedback in the following manner: the voltage across the emitter resistor, which is proportional to the collector

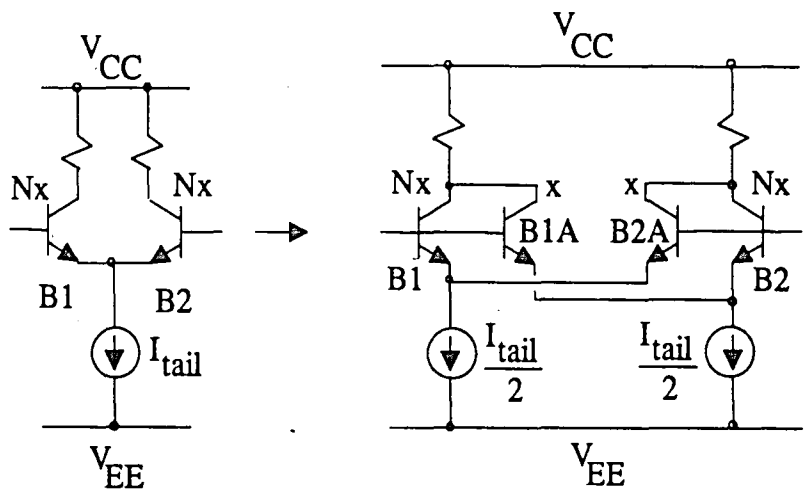


Figure 18. Input Stage Modification To Reduce Transconductance

current, subtracts directly from the base-emitter voltage. In the input configuration used in the circuit, changes in the base-emitter voltage of B1 cause less of a change in the total collector current of B1 and B1A because transistor B1A gets its emitter current

from another current source. With the scaling of x and Nx used in Figure 18, the effective reduction in transconductance can be calculated to be:

$$\text{transconductance reduction factor} = \frac{(1+N)^2}{4N} \qquad (3.9)$$

where N is the ratio of the large emitter area to the small emitter area. For this design, a value of N equal to three was chosen as a compromise through simulation.

Some additional comments about the input stage used are appropriate. Diode connected devices B3 and B4 allow headroom for operation of the second stage current source. Resistors RC3 and RC4 and capacitors C3 and C4 are used as secondary compensation elements to control stability at high frequencies, which will be explained in more detail later. Finally, two current sources sourcing 4 mA each are used, equivalent in effect to a single 8 mA tail current. This current level would be considered high for a general purpose op amp, but is appropriate for achieving low noise performance. An undesirable side-effect of using such a large tail current is the corresponding increase in input bias current. The addition of input bias current cancellation circuitry can adversely affect noise performance and is usually not an option. A decision was made early on to use NPN input devices because their β is greater than that of PNP devices.

The second gain stage is comprised of PNP devices B10 and B11 connected in a common emitter configuration with transistor B12 and resistor R8 acting as a 4 mA current source and devices B13 and B14 acting as a current mirror/active load. Emitter degeneration resistors R12 and R13 act to both reduce voltage offset and increase slew rate. Differential-to-single-ended conversion also occurs at this stage, the output being at the collector of B14. Symmetrical capacitors and resistors C1, C2, R6 and R7 provide

primary high frequency compensation for the circuit, effectively killing the gain of devices B10 and B11 at frequencies above the location of the primary pole.

All components to the right of B15 in the schematic of Figure 17 comprise a unity gain output buffer stage. Transistors B19 and B20 are the main current driving devices of this class AB push-pull output stage, scaled to provide at least 50 mA of current drive while still maintaining reasonable betas. Devices B15 and B16, biased by 5 mA current sources made up of B17 and R9, and B18 and R10, eliminate crossover distortion. The quiescent current through B19 and B20 is determined by the values of the current sources feeding B15 and B16 as well as the emitter area scaling of B15 and B16. This can be seen by inspection of the following voltage loop:

$$V_{BE,B15} + V_{BE,B16} = V_{BE,B19} + V_{BE,B20} \qquad (3.10)$$

The following relationship exists between collector current and base-to-emitter voltage:

$$V_{BE} = V_T \ln \frac{I_C}{I_S} \qquad (3.11)$$

$$\text{where: } V_T = \frac{kT}{q}$$

Substitution of Equation (3.11) into Equation (3.10) yields:

$$V_T \ln\left[\frac{I_{C,B15}}{I_{S,B15}}\frac{I_{C,B16}}{I_{S,B16}}\right] = V_T \ln\left[\frac{I_{C,B19}}{I_{S,B19}}\frac{I_{C,B20}}{I_{S,B20}}\right] \qquad (3.12)$$

In the quiescent state, the collector currents of B19 and B20 are equal. The collector currents of B15 and B16 are made equal by using the same forced value for each current

source feeding them. Simplifying and solving for the quiescent collector current of B19 and B20, the following result is obtained:

$$I_{C,B19} = I_{C,B20} = \sqrt{\left({I_{C,B15}}^2 \frac{I_{S,B19} I_{S,B20}}{I_{S,B15} I_{S,B16}} \right)} \qquad (3.13)$$

The saturation current for a transistor can be represented as:

$$I_S = AJ \qquad (3.14)$$

where: A = emitter area

J = current density

It should be noted that the current densities and therefore saturation currents of NPN and PNP devices are different. Hence, by choosing an appropriate value for the current sources feeding B15 and B16, and by properly scaling the emitter areas of all four transistors which in turn determines the saturation currents of each device, a desired quiescent collector current for the output stage can be obtained. Values for saturation current are denoted by I_S in the model parameter listing in Appendix A. Substitution of the appropriate model parameters into Equation (3.13) yields a collector current of 2.07 mA, close to the 2.34 mA resulting from simulations.

Attention must be paid to potential breakdown problems in the output stage presented. The collector-to-emitter breakdown voltage should not exceed 8V, and since the circuit is designed for a +/- 3V output voltage swing, an analysis must be done to ensure that this limit is never exceeded. Output devices B19 and B20 will be at the limit of this breakdown at each voltage extreme, so the design presented will function

properly as long as the recommended output voltage range is not exceeded. Because transistors B15 and B16 alone would exceed the breakdown limit by a V_{BE} at each voltage extreme, diode-connected devices B15B and B16B are added.

The small-valued series resistor R11 provides some passive current-limiting and also decreases peaking of the closed loop response when loads with inductive or capacitive components are being driven.

The output drive current capability of the output stage shown is dependent on two factors. The first factor is the current-handling capability of the main output transistors B19 and B20. Since a single NV663A01 or PV693A01 device will drive 30 mA maximum, scaled by two they will be capable of driving somewhere around 60 mA. The other factor requires that the needed base current is available to drive both of these devices when worst-case betas are considered. Since most of the 4 mA available from current sources B17 and B18 will drive the bases of B19 and B20 respectively, a worst case beta of 15 ensures that 60 mA of collector current will flow if necessary.

Optimizing the given op amp architecture to achieve the best AC performance requires making choices regarding tradeoffs which finally result in a balance of compromises. Design goals which include unity gain stability, low noise, high gain bandwidth, high slew rate, high open loop gain, low offsets and low supply current generally work against each other.

A qualitative description of some key AC parameters follows. The unity gain configuration is the most difficult one in terms of stability. To compensate for unity gain, a large enough capacitance must be placed in the circuit in a location where its increasing impedance will act to kill gain at higher frequencies. Because this capacitance

is often the element which limits the slew rate of the amplifier, it is desirable to keep this capacitance as low as possible. A side effect of increasing the capacitance to be large enough to achieve stability is a proportional decrease in the gain of the amplifier at higher frequencies, thereby also adversely affecting the level of input-referred noise.

The only way to attack this parametrical tug of war is to make some baseline decisions on specific parameters and live with the effects of these constraints on the remaining parameters. A fundamental constraint also requires that all necessary circuit components such as compensation capacitors be available on the array. This of course would not be a factor for a full custom design. Three key parameters were chosen to be absolutely necessary: maintaining an input-referred noise level below $1nV/\sqrt{Hz}$, attaining a phase margin of at least 45 degrees with a positive gain margin and achieving a gain bandwidth product of at least 300 MHz. All other parameters were optimized as best as possible without compromising these three requirements.

The compensation scheme as shown in Figure 17 uses two sets of compensation networks. Primary compensation is provided by capacitors C1 and C2 which act to kill second stage gain starting at the primary or low frequency pole. Series resistors R6 and R7 add a zero to the response which effectively helps to control the location and steepness of the phase response change. Secondary compensation is controlled by capacitors C3 and C4 in the input stage. Resistors RC3 and RC4 add zeroes to the magnitude response near the unity gain point, reshaping the phase response to change more abruptly yet at a higher frequency. The gain bandwidth product and slew rate are inversely proportional to the size of compensation capacitance used. In general, the gain bandwidth product is proportional to the transconductance of the input stage and inversely proportional to the value of compensation capacitance used. The slew rate is

equal to the current available to charge the capacitance divided by the capacitance itself. A textbook analysis of these parameters typically assumes compensation at the point where the differential-to-single-ended conversion is done. Compensation for this particular circuit occurs differentially before this conversion is accomplished.

IV. SIMULATION RESULTS

Qualitative analysis and hand calculations are vital practices necessary for defining the topology and approximate component values of any circuit, but computer simulations are needed to verify any design before committing to the start of a costly fabrication process. All simulations were performed using AT&T's ADVICE simulator on a SUN workstation.

A summary of DC parameters simulated using nominal processing models is shown in tabular form in Figure 19. Appendix A lists all of the unscaled nominal processing device models used in the simulations.

Appendix C contains simulation results for the op amp, including a summary of total input-referred noise and a listing of noise contributions from the input devices . The noise contribution of each component is shown as the last value on each line in units of volts squared per hertz. For bipolar junction transistors, these components are further broken down into contributions from thermal noise (RB, RC and RE), shot noise (IB and IC) and parasitic diode noise (PD). Flicker noise (FN) is not included because the flicker noise coefficient is set to zero. Only detailed noise contributions from the input devices are shown for brevity, although the final noise summary includes noise contributions from all components, including parasitic components. These values at the end of each line add directly to yield a total output noise voltage for the amplifier which is then divided by a transfer function gain to yield a value for equivalent input noise, that

PARAMETER	NOMINAL VALUE	UNITS
input offset voltage	+1.600	mV
input bias current	+26.960	uA
input offset current	+1.194	uA
(+)cmrr	-66.076	dB
(-)cmrr	-65.283	dB
VCC current	21.141	mA
VEE current	-21.195	mA
(+)psrr	-69.642	dB
(-)psrr	-74.249	dB
(+)open loop gain	+65.094	dB
(-)open loop gain	+66.015	dB

Figure 19. Summary of Simulated DC Parameters

value being 0.7972 $nV/\sqrt{Hz}$. The noise analysis is performed at a frequency of 10 KHz, although the input-referred noise remains constant until gain rolloff occurs above the unity gain frequency of approximately 300 MHz. The noise current of the amplifier was simulated and found to be 2.05 $pA/\sqrt{Hz}$.

Figures 20 and 21 indicate the output current drive capability of the op amp. Figure 20 indicates that when the amplifier is set up in a follower configuration with a DC input voltage of +3 V, the amplifier is capable of driving 60 mA into a 50 ohm load. Figure 21 shows the same result when an input voltage of - 3V is applied.

Because package parasitics can greatly affect a design's performance, especially at higher frequencies, they should always be included in the simulation process. A schematic of the package parasitics used in the simulation of the low noise op amp is shown in Figure 22. It assumes an eight pin small outline integrated circuit (SOIC) package is used. The connection from the IC pad to the end of the package pin consists of inductances due to a bonding wire (Lwire), a leadframe trace (Ltrace) and an exposed part of the package pin itself (Llead). Capacitances from each connection point to ground are also included. Package pin functionality assignment was done to match the industry standard pinout for a single op amp.

A graph of loop gain magnitude and phase versus frequency is shown in Figure 23, indicating the circuit has a gain bandwidth product of 309.8 MHz with 55.25 degrees of phase margin and 4.92 dB of gain margin. This simulation was performed in a unity gain configuration. As external gains become higher, stability will improve. The actual simulator output text is included in Appendix C.

The closed loop response of the amplifier in a unity gain configuration is shown in Figure 24, indicating minimal peaking (less than 0.4 dB). Both magnitude and phase versus frequency are shown.

Figure 25 reveals the transient response of the amplifier, indicating an output voltage overshoot of less than 0.1 V for a -1 V to +1 V input voltage step. The slew rate is approximately 85 V/uS for both positive-going and negative-going waveforms. This is not spectacular speed, especially for CBIC-V technology, but is acceptable considering the limitations imposed by other requirements including low noise and unity gain stability.

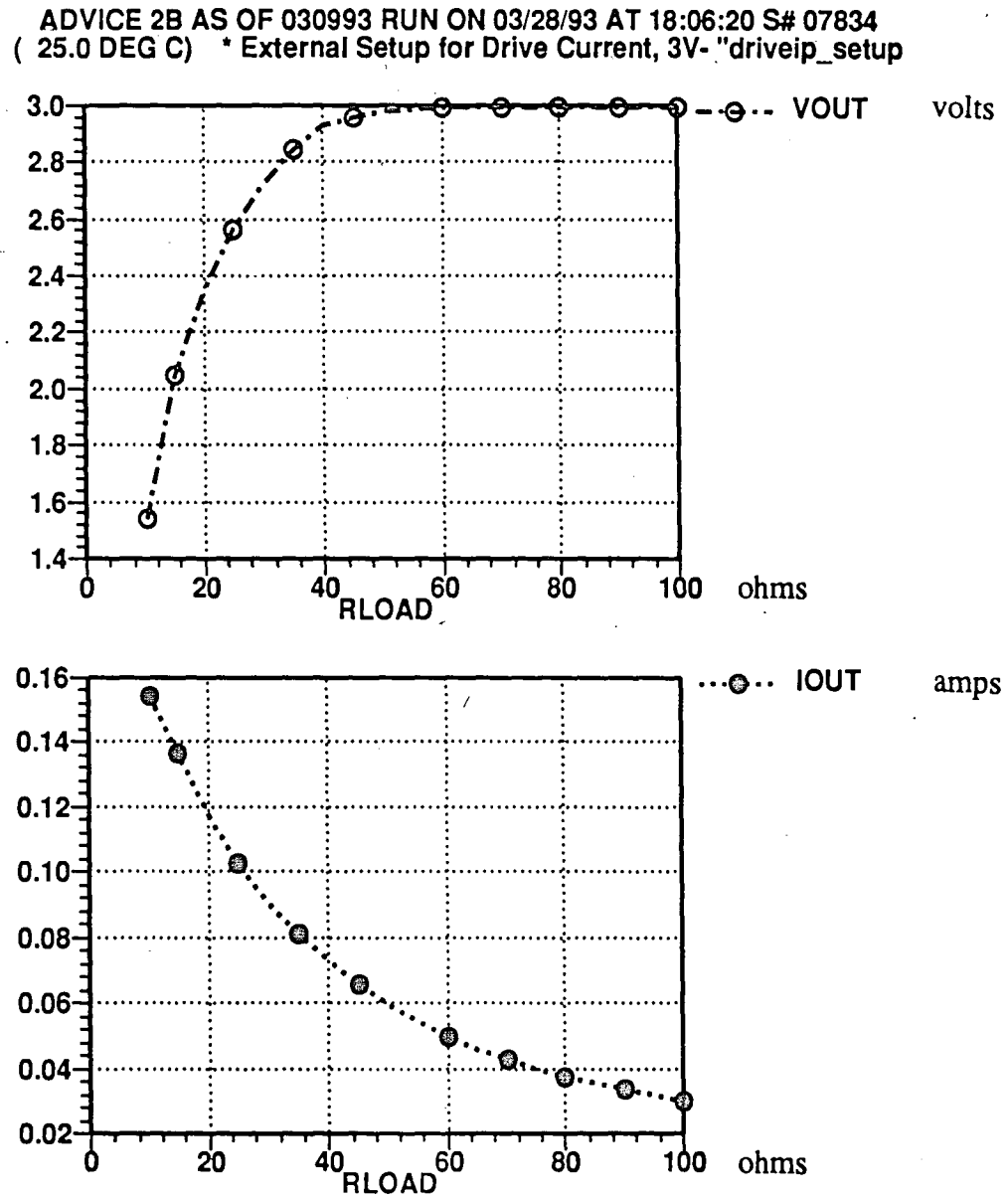


Figure 20. Output Drive Current Capability, +3 V Input Voltage

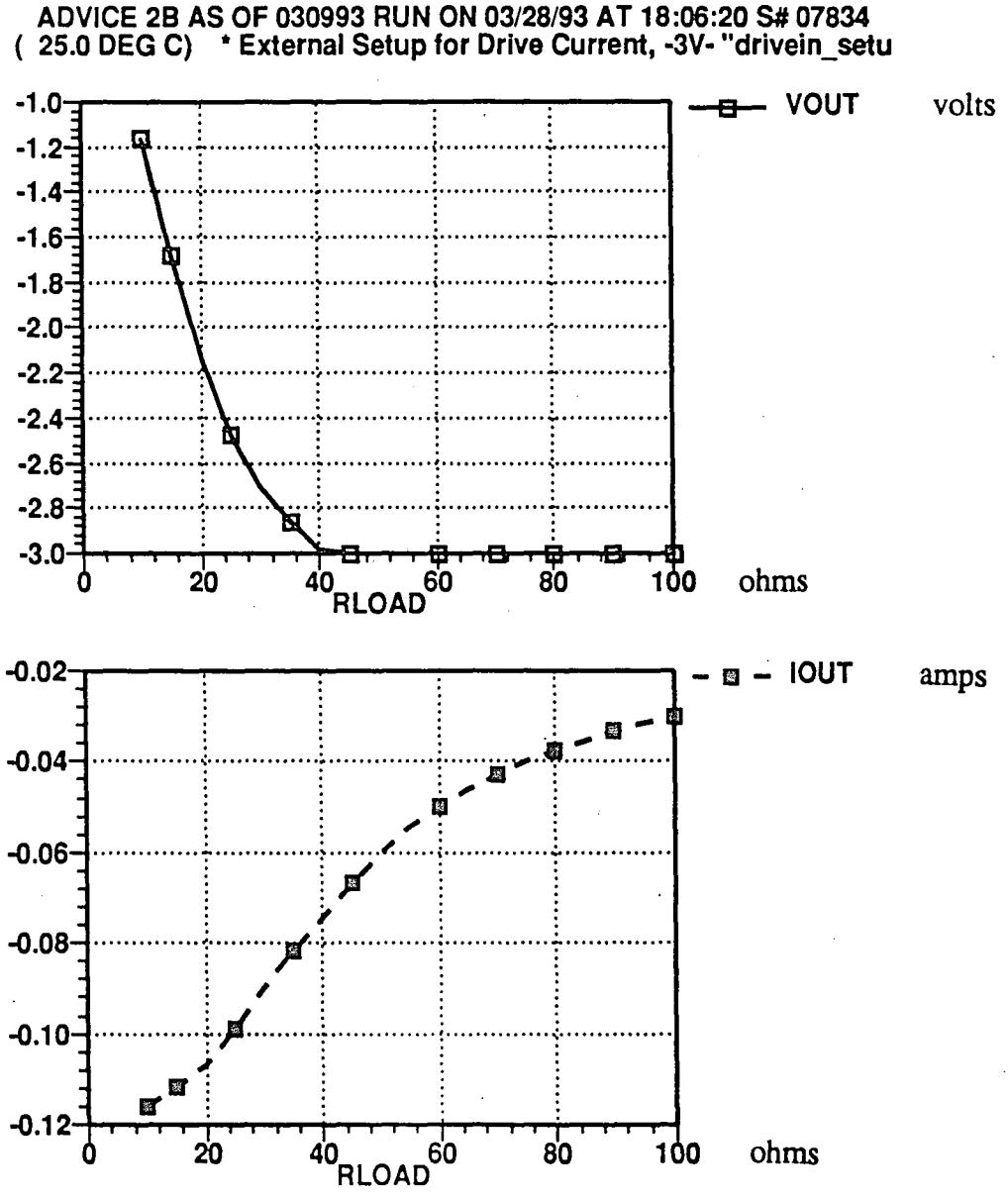
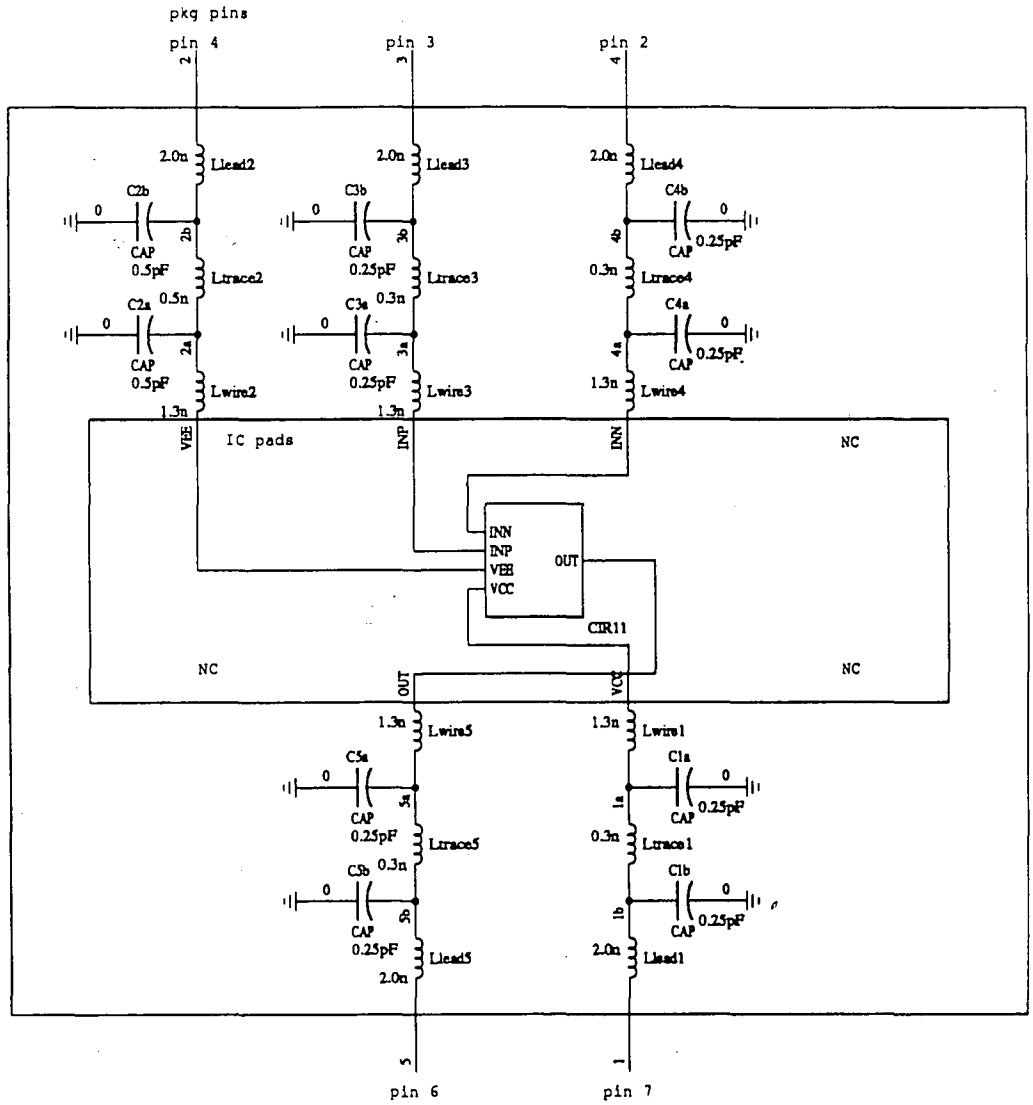


Figure 21. Output Drive Current Capability, -3 V Input Voltage



Package Parasitics, 8 pin SOIC

Figure 22. Schematic of Package Parasitics

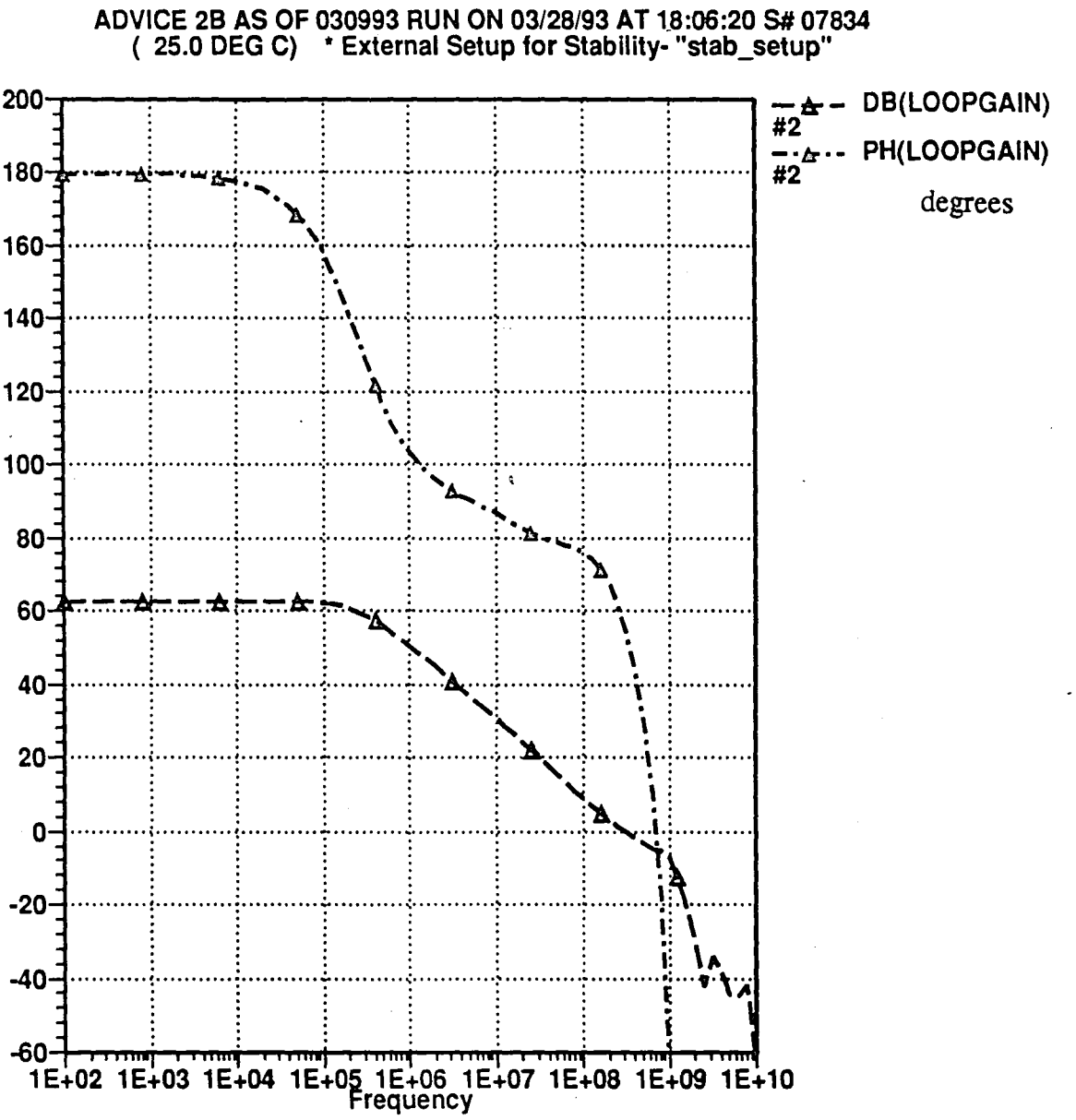


Figure 23. Loop Gain Magnitude And Phase Plot

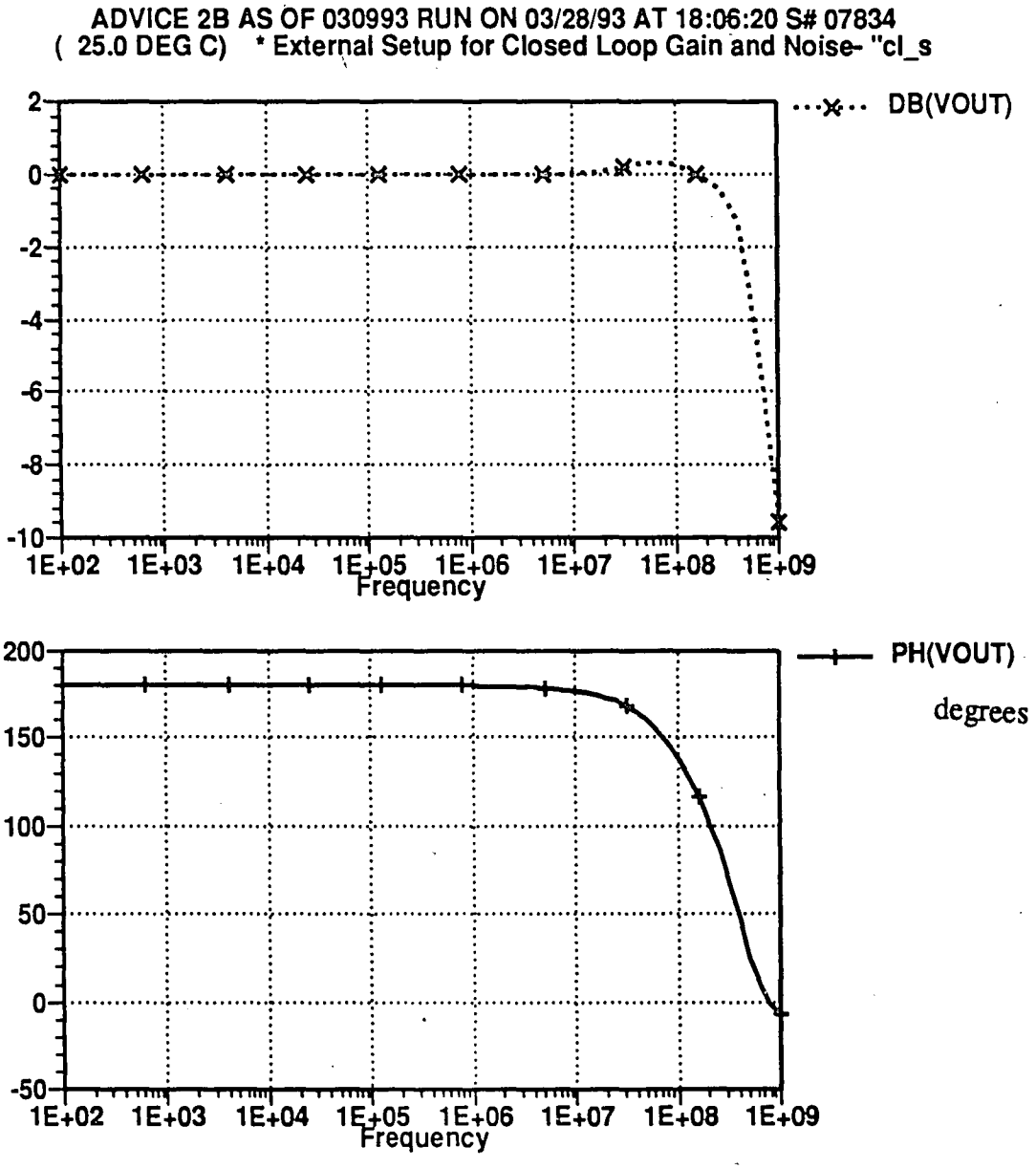


Figure 24. Closed Loop Gain Magnitude And Phase Plot

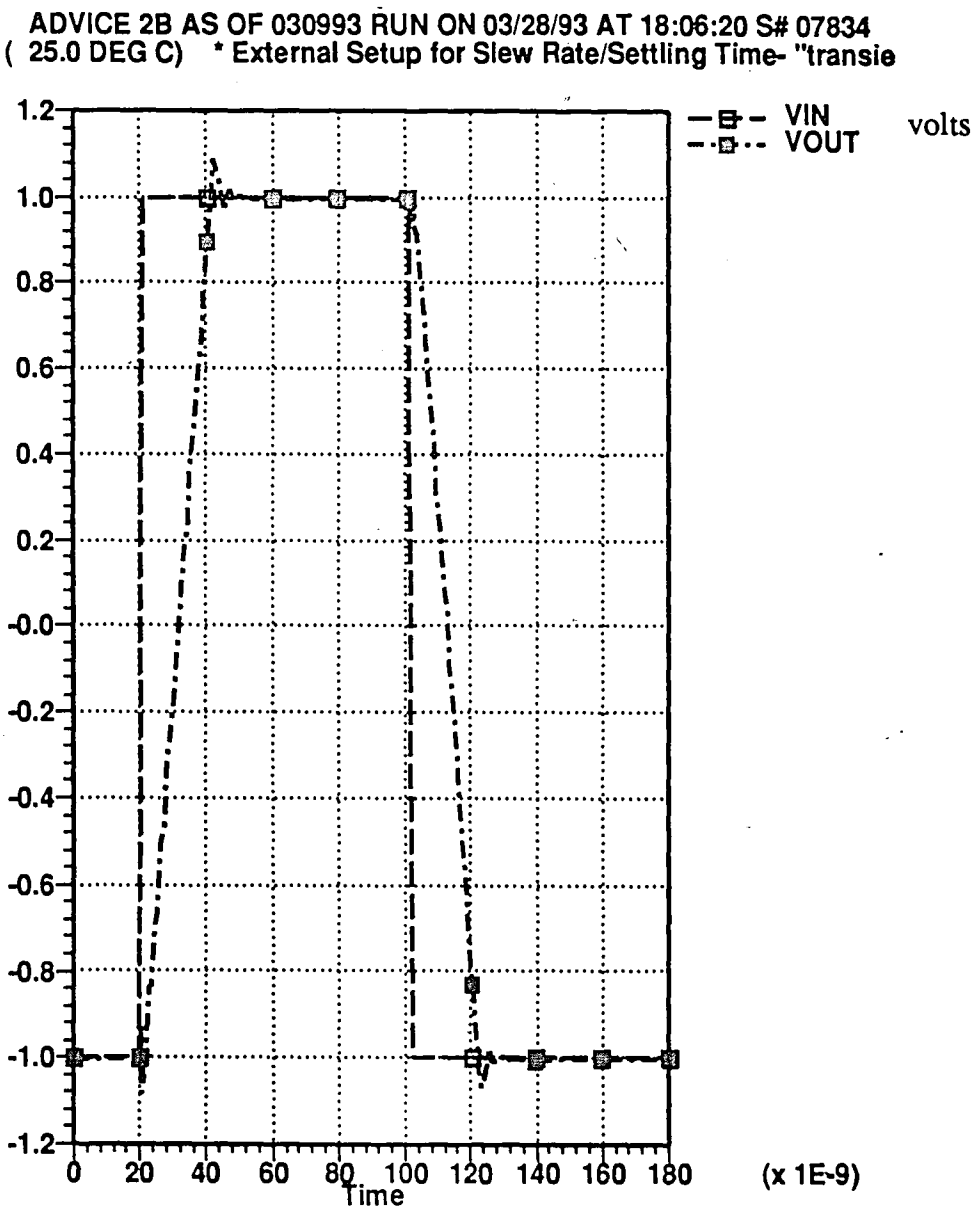


Figure 25. Transient Response Plot

Appendix C also contains results of a simulation performed to reveal total harmonic distortion (THD). A THD analysis consists of a Fourier analysis that fits the leading components of a Fourier series to a specified transient waveform, in this case a sine wave. The simulation performed indicates a total harmonic distortion of 0.006% when driving a 1 MHz, 2 V peak amplitude sine wave (-2V to + 2 V) into a load of 50 ohms in parallel with 2 pF. This THD number represents the RMS sum of the normalized magnitudes of the second through ninth-order Fourier coefficients.

V. CONCLUSION

Many systems today require low noise front end amplification. The design process presented here has attempted to indoctrinate the reader to some of the challenges faced by the designer of a general purpose low noise operational amplifier. The inability to place adequate gain in the input stage of a current mode feedback amplifier precludes its use as a viable low noise architecture, pointing to a voltage feedback solution instead. The straightforward approach presented makes modifications to a classic voltage feedback op amp architecture yielding excellent results for the chosen target parameters of input-referred voltage noise, bandwidth and unity gain stability.

Types of noise were discussed and relevant concepts were presented including noise modeling in an amplifier, noise in cascaded gain stages, a simple voltage feedback arrangement and the physical sources of noise in a real transistor. Results from the initial analysis of a simple input stage indicated the feasibility of attaining the required specifications and also served as a best case baseline that provided the designer a reference point from which to judge performance changes as the design evolved.

Clearly, a requirement for low input-referred noise places great demands on both the process technology used as well as the actual design. To achieve the low noise specifications, devices with low base resistance must be available. To achieve high gain bandwidth those same devices must possess a high f_T frequency. The architecture used

should place adequate gain in the front end to minimize the effects of later stages on the input-referred noise.

Reduction of the transconductance of the input devices, besides extending the allowable input signal and linearity range, also increases slew rate by reducing the size of the compensation capacitance required to achieve stability. Since the addition of emitter degeneration resistors (a traditional method of reducing transconductance) would have introduced a severe noise penalty, an emitter current stealing technique was used. The input stage chosen used NV431A01 devices, each with a scale factor of 4 where one quarter of the emitter area was used to steal current for transconductance reduction. The simulation models for all devices, including the NV431A01 with a scale factor of unity, are detailed in Appendix A.

Design of the second gain stage and the output stage, although less critical from a noise standpoint, focused on many issues including frequency compensation and power supply current minimization. The latter was accomplished by reduction of the quiescent output stage current.

A large amount of source material exists pertaining to the sources of electrical noise and techniques for optimizing noise performance. The concepts presented here are only a small subset of that much larger body of knowledge. Successful low noise design requires not only an understanding of basic principles, but also an appreciation of each parameter's relative importance, thereby allowing a designer to balance the compromises to be made.

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APPENDICES

APPENDIX A

Nominal Models for ADVICE-

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* LIBRARY UPDATE VERSION 93.1 2/2/93 15:19:09

* CBIC-V LIBRARY CREATED Wed Nov 27 17:15:00 EST 1991
* ADVANCED CBIC-V Models with improved scaling from the "231" device
*
* STANDARD CBIC-V LIBRARY SCALED FROM "231" MODEL - RDP
* FOR USE WITH ADVICE ADMIT (USER-DEFINED) 4-TERM G-P MODEL
**
** STANDARD SUPPORTED DEVICES
**

MOD_NV231A01   728684373  96   200  100660 1355

 **
 **
* TWO 1.5 BY 15 MICRON STRIPES - NOM
**                                JDJ/RDP 11/11/91
**
.MODEL NV231A01 USRMOD=NEB1 % NPN NOM  MODEL,
 + RBX = 2.500E+01  RBI = 2.783E+01  RCX = 1.967E+01  RCI = 4.427E+01
 + RE  = 1.945E+00  IS  = 1.420E-16  I1  = 5.800E-19  I2  = 5.108E-14
 + NE  = 2.000E+00  IK  = 9.714E-03  VBO = 1.320E+00  TFO = 3.900E-12
 + CJE = 1.200E-13  PE  = 8.000E-01  ME  = 4.950E-01  BE  = 1.000E-01
 + I3  = 1.502E-16  I4  = 6.444E-21  NC  = 1.847E+00  IKR = 8.172E-02
 + VAO = 7.901E+00  TRO = 4.000E-11  CJC = 6.670E-15  PC  = 6.701E-01
 + MC  = 4.509E-01  BC  = 1.000E-01  EA  = 1.184E+00  DEA = 6.825E-02
 + TO  = 2.500E+01  KFN = 0.000E+00  AFN = 1.000E+00  BFN = 1.000E+00
 + BVBC= 0.000E+00  ALC1= 2.000E+00  ALC2= 0.000E+00  ALTC= 7.500E-01
 + BVBE= 0.000E+00  ALE1= 2.000E+00  ALE2= 0.000E+00  ALTE= 7.500E-01
 + NID = 8.197E-12  QCO = 1.744E-14  VJCO= 9.055E-01  TRCI= 2.000E+00
 + TVCO= 1.680E+00  RBIP= 8.042E+01  I1P = 7.500E-20  I2P = 1.000E-14
 + NEP = 1.313E+00  IKP = 3.000E-03  CJEP= 7.183E-14  ISP = 1.285E-18
 + I3P = 9.069E-18  CJCP= 1.016E-13  PS  = 5.335E-01  MS  = 4.389E-01
 + BS  = 1.000E-01  MTQB= 1.103E+00  DEA2= 5.615E-02  XTIS= 2.000E+00
 + XTI1= 3.000E+00  XTI2= 2.500E+00  QCOX= 8.722E-14  NR  = 1.020E+00
 + NF  = 1.002E+00  NCR = 1.090E+00  NCRP= 1.000E+00  MVC1= 1.000E-01


MOD_NV431A01   728684382  96   200  100660 1356

 **
 **
* FOUR 1.5 BY 15 MICRON STRIPES - NOM
```

```
**                                JDJ/RDP 11/11/91
**
.MODEL NV431A01 USRMOD=NEB1 % NPN NOM  MODEL
+ RBX = 1.250E+01  RBI = 1.391E+01  RCX = 3.002E+01  RCI = 2.213E+01
+ RE  = 9.725E-01  IS  = 2.840E-16  I1  = 1.160E-18  I2  = 1.022E-13
+ NE  = 2.000E+00  IK  = 1.943E-02  VBO = 1.320E+00  TFO = 3.900E-12
+ CJE = 2.400E-13  PE  = 8.000E-01  ME  = 4.950E-01  BE  = 1.000E-01
+ I3  = 3.004E-16  I4  = 1.289E-20  NC  = 1.847E+00  IKR = 1.634E-01
+ VAO = 7.901E+00  TRO = 4.000E-11  CJC = 1.334E-14  PC  = 6.701E-01
+ MC  = 4.509E-01  BC  = 1.000E-01  EA  = 1.184E+00  DEA = 6.825E-02
+ TO  = 2.500E+01  KFN = 0.000E+00  AFN = 1.000E+00  BFN = 1.000E+00
+ BVBC= 0.000E+00  ALC1= 2.000E+00  ALC2= 0.000E+00  ALTC= 7.500E-01
+ BVBE= 0.000E+00  ALE1= 2.000E+00  ALE2= 0.000E+00  ALTE= 7.500E-01
+ NID = 8.197E-12  QCO = 2.442E-14  VJCO= 9.055E-01  TRCI= 2.000E+00
+ TVCO= 1.680E+00  RBIP= 4.650E+01  I1P = 1.320E-19  I2P = 1.760E-14
+ NEP = 1.313E+00  IKP = 5.280E-03  CJEP= 1.242E-13  ISP = 2.019E-18
+ I3P = 1.596E-17  CJCP= 1.491E-13  PS  = 5.335E-01  MS  = 4.389E-01
+ BS  = 1.000E-01  MTQB= 1.103E+00  DEA2= 5.615E-02  XTIS= 2.000E+00
+ XTI1= 3.000E+00  XTI2= 2.500E+00  QCOX= 1.221E-13  NR  = 1.020E+00
+ NF  = 1.002E+00  NCR = 1.090E+00  NCRP= 1.000E+00  MVC1= 1.000E-01


MOD_NV362A01   728684387  96   200   100660 1357

**
**
* THREE 1.5 BY 30 MICRON STRIPES - NOM
**                                JDJ/RDP 11/11/91
**
.MODEL NV362A01 USRMOD=NEB1 % NPN NOM  MODEL
+ RBX = 8.423E+00  RBI = 9.377E+00  RCX = 5.737E+00  RCI = 1.492E+01
+ RE  = 6.553E-01  IS  = 4.214E-16  I1  = 1.721E-18  I2  = 1.516E-13
+ NE  = 2.000E+00  IK  = 2.883E-02  VBO = 1.320E+00  TFO = 3.900E-12
+ CJE = 3.561E-13  PE  = 8.000E-01  ME  = 4.950E-01  BE  = 1.000E-01
+ I3  = 4.458E-16  I4  = 1.913E-20  NC  = 1.847E+00  IKR = 2.425E-01
+ VAO = 7.901E+00  TRO = 4.000E-11  CJC = 1.980E-14  PC  = 6.701E-01
+ MC  = 4.509E-01  BC  = 1.000E-01  EA  = 1.184E+00  DEA = 6.825E-02
+ TO  = 2.500E+01  KFN = 0.000E+00  AFN = 1.000E+00  BFN = 1.000E+00
+ BVBC= 0.000E+00  ALC1= 2.000E+00  ALC2= 0.000E+00  ALTC= 7.500E-01
+ BVBE= 0.000E+00  ALE1= 2.000E+00  ALE2= 0.000E+00  ALTE= 7.500E-01
+ NID = 8.197E-12  QCO = 3.662E-14  VJCO= 9.055E-01  TRCI= 2.000E+00
+ TVCO= 1.680E+00  RBIP= 3.415E+01  I1P = 1.818E-19  I2P = 2.424E-14
+ NEP = 1.313E+00  IKP = 7.272E-03  CJEP= 1.691E-13  ISP = 1.303E-18
+ I3P = 2.198E-17  CJCP= 2.174E-13  PS  = 5.335E-01  MS  = 4.389E-01
+ BS  = 1.000E-01  MTQB= 1.103E+00  DEA2= 5.615E-02  XTIS= 2.000E+00
+ XTI1= 3.000E+00  XTI2= 2.500E+00  QCOX= 1.832E-13  NR  = 1.020E+00
+ NF  = 1.002E+00  NCR = 1.090E+00  NCRP= 1.000E+00  MVC1= 1.000E-01


MOD_NV663A01   728684395  96   200   100660 1355
```

```
**
**
* SIX 1.5 BY 30 MICRON STRIPES - NOM
**                                JDJ/RDP 11/11/91
**
.MODEL NV663A01 USRMOD=NEB1 % NPN NOM  MODEL
+ RBX = 4.212E+00  RBI = 4.689E+00  RCX = 2.869E+00  RCI = 7.458E+00
+ RE  = 3.277E-01  IS  = 8.429E-16  I1  = 3.443E-18  I2  = 3.032E-13
+ NE  = 2.000E+00  IK  = 5.766E-02  VBO = 1.320E+00  TFO = 3.900E-12
+ CJE = 7.123E-13  PE  = 8.000E-01  ME  = 4.950E-01  BE  = 1.000E-01
+ I3  = 8.916E-16  I4  = 3.825E-20  NC  = 1.847E+00  IKR = 4.851E-01
+ VAO = 7.901E+00  TRO = 4.000E-11  CJC = 3.959E-14  PC  = 6.701E-01
+ MC  = 4.509E-01  BC  = 1.000E-01  EA  = 1.184E+00  DEA = 6.825E-02
+ TO  = 2.500E+01  KFN = 0.000E+00  AFN = 1.000E+00  BFN = 1.000E+00
+ BVBC= 0.000E+00  ALC1= 2.000E+00  ALC2= 0.000E+00  ALTC= 7.500E-01
+ BVBE= 0.000E+00  ALE1= 2.000E+00  ALE2= 0.000E+00  ALTE= 7.500E-01
+ NID = 8.197E-12  QCO = 4.709E-14  VJCO= 9.055E-01  TRCI= 2.000E+00
+ TVCO= 1.680E+00  RBIP= 1.708E+01  I1P = 3.636E-19  I2P = 4.848E-14
+ NEP = 1.313E+00  IKP = 1.454E-02  CJEP= 3.383E-13  ISP = 2.607E-18
+ I3P = 4.397E-17  CJCP= 3.879E-13  PS  = 5.335E-01  MS  = 4.389E-01
+ BS  = 1.000E-01  MTQB= 1.103E+00  DEA2= 5.615E-02  XTIS= 2.000E+00
+ XTI1= 3.000E+00  XTI2= 2.500E+00  QCOX= 2.355E-13  NR  = 1.020E+00
+ NF  = 1.002E+00  NCR = 1.090E+00  NCRP= 1.000E+00  MVC1= 1.000E-01


**********************************************************************
!<arch>
MOD_PV111A01   728684699  96   200  100660 1679
* LIBRARY UPDATE VERSION 93.1 2/2/93 15:24:46
* CBIC-V LIBRARY CREATED Wed Nov 27 17:15:00 EST 1991
* ADVANCED CBIC-V Models with improved scaling from the "231" device
*
* STANDARD CBIC-V LIBRARY SCALED FROM "231" MODEL - RDP
* FOR USE WITH ADVICE ADMIT (USER-DEFINED) 4-TERM G-P MODEL
**
** STANDARD SUPPORTED DEVICES
**

MOD_PV231A01   728684707  96   200  100660 1355

 **
 **
* TWO 1.5 BY 15 MICRON STRIPES - NOM
**                                JDJ/RDP 11/19/91
**
.MODEL PV231A01 USRMOD=PEB1 % PNP NOM  MODEL
+ RBX = 1.447E+01  RBI = 1.933E+01  RCX = 9.156E+01  RCI = 9.067E+01
+ RE  = 1.276E+00  IS  = 1.051E-16  I1  = 7.800E-19  I2  = 2.676E-15
+ NE  = 1.459E+00  IK  = 8.847E-03  VBO = 8.500E-01  TFO = 4.500E-12
```

```
+ CJE = 1.200E-13 PE = 7.351E-01 ME = 4.930E-01 BE = 8.922E-02
+ I3 = 1.700E-18 I4 = 7.541E-16 NC = 1.700E+00 IKR = 1.000E-01
+ VAO = 2.958E+00 TRO = 1.500E-10 CJC = 1.068E-14 PC = 7.771E-01
+ MC = 5.000E-01 BC = 1.000E-01 EA = 1.184E+00 DEA = 6.825E-02
+ TO = 2.500E+01 KFN = 0.000E+00 AFN = 1.000E+00 BFN = 1.000E+00
+ BVBC= 0.000E+00 ALC1= 2.000E+00 ALC2= 0.000E+00 ALTC= 7.500E-01
+ BVBE= 0.000E+00 ALE1= 2.000E+00 ALE2= 0.000E+00 ALTE= 7.500E-01
+ NID = 2.932E-12 QCO = 3.000E-14 VJCO= 1.498E+00 TRCI= 2.000E+00
+ TVCO= 1.680E+00 RBIP= 5.000E+01 I1P = 5.575E-18 I2P = 1.475E-15
+ NEP = 1.722E+00 IKP = 1.154E-02 CJEP= 1.149E-13 ISP = 7.525E-18
+ I3P = 5.000E-17 CJCP= 5.080E-13 PS = 9.082E-01 MS = 4.931E-01
+ BS = 1.000E-01 MTQB= 1.050E+00 DEA2= 1.778E-01 XTIS= 2.000E+00
+ XTI1= 3.000E+00 XTI2= 2.200E+00 QCOX= 1.500E-13 NFP = 1.000E+00
+ NF = 1.000E+00 NCR = 1.000E+00 NCRP= 1.000E+00 NR = 1.000E+00


MOD_PV432A01  728684716  96  200  100660 1356

**
**
* FOUR 1.5 BY 15 MICRON STRIPES - NOM
**                                JDJ/RDP 11/19/91
**
.MODEL PV432A01 USRMOD=PEB1 % PNP NOM MODEL
+ RBX = 7.235E+00 RBI = 9.665E+00 RCX = 5.180E+01 RCI = 4.533E+01
+ RE = 6.380E-01 IS = 2.102E-16 I1 = 1.560E-18 I2 = 5.352E-15
+ NE = 1.459E+00 IK = 1.769E-02 VBO = 8.500E-01 TFO = 4.500E-12
+ CJE = 2.400E-13 PE = 7.351E-01 ME = 4.930E-01 BE = 8.922E-02
+ I3 = 3.400E-18 I4 = 1.508E-15 NC = 1.700E+00 IKR = 2.000E-01
+ VAO = 2.958E+00 TRO = 1.500E-10 CJC = 2.136E-14 PC = 7.771E-01
+ MC = 5.000E-01 BC = 1.000E-01 EA = 1.184E+00 DEA = 6.825E-02
+ TO = 2.500E+01 KFN = 0.000E+00 AFN = 1.000E+00 BFN = 1.000E+00
+ BVBC= 0.000E+00 ALC1= 2.000E+00 ALC2= 0.000E+00 ALTC= 7.500E-01
+ BVBE= 0.000E+00 ALE1= 2.000E+00 ALE2= 0.000E+00 ALTE= 7.500E-01
+ NID = 2.932E-12 QCO = 3.923E-14 VJCO= 1.498E+00 TRCI= 2.000E+00
+ TVCO= 1.680E+00 RBIP= 2.891E+01 I1P = 9.812E-18 I2P = 2.596E-15
+ NEP = 1.722E+00 IKP = 2.031E-02 CJEP= 1.987E-13 ISP = 9.782E-18
+ I3P = 8.800E-17 CJCP= 8.300E-13 PS = 9.082E-01 MS = 4.931E-01
+ BS = 1.000E-01 MTQB= 1.050E+00 DEA2= 1.778E-01 XTIS= 2.000E+00
+ XTI1= 3.000E+00 XTI2= 2.200E+00 QCOX= 1.962E-13 NFP = 1.000E+00
+ NF = 1.000E+00 NCR = 1.000E+00 NCRP= 1.000E+00 NR = 1.000E+00


MOD_PV392A01  728684725  96  200  100660 1357

**
**
* THREE 1.5 BY 45 MICRON STRIPES - NOM
**                                JDJ/RDP 11/19/91
**
```

```
.MODEL PV392A01 USRMOD=PEB1 % PNP NOM  MODEL
+ RBX = 3.262E+00 RBI = 4.358E+00 RCX = 2.189E+01 RCI = 2.044E+01
+ RE  = 2.877E-01 IS  = 4.662E-16 I1  = 3.460E-18 I2  = 1.187E-14
+ NE  = 1.459E+00 IK  = 3.924E-02 VBO = 8.500E-01 TFO = 4.500E-12
+ CJE = 5.323E-13 PE  = 7.351E-01 ME  = 4.930E-01 BE  = 8.922E-02
+ I3  = 7.541E-18 I4  = 3.345E-15 NC  = 1.700E+00 IKR = 4.436E-01
+ VAO = 2.958E+00 TRO = 1.500E-10 CJC = 4.737E-14 PC  = 7.771E-01
+ MC  = 5.000E-01 BC  = 1.000E-01 EA  = 1.184E+00 DEA = 6.825E-02
+ TO  = 2.500E+01 KFN = 0.000E+00 AFN = 1.000E+00 BFN = 1.000E+00
+ BVBC= 0.000E+00 ALC1= 2.000E+00 ALC2= 0.000E+00 ALTC= 7.500E-01
+ BVBE= 0.000E+00 ALE1= 2.000E+00 ALE2= 0.000E+00 ALTE= 7.500E-01
+ NID = 2.932E-12 QCO = 6.231E-14 VJCO= 1.498E+00 TRCI= 2.000E+00
+ TVCO= 1.680E+00 RBIP= 1.495E+01 I1P = 1.933E-17 I2P = 5.115E-15
+ NEP = 1.722E+00 IKP = 4.002E-02 CJEP= 3.843E-13 ISP = 7.632E-18
+ I3P = 1.734E-16 CJCP= 1.431E-12 PS  = 9.082E-01 MS  = 4.931E-01
+ BS  = 1.000E-01 MTQB= 1.050E+00 DEA2= 1.778E-01 XTIS= 2.000E+00
+ XTI1= 3.000E+00 XTI2= 2.200E+00 QCOX= 3.115E-13 NFP = 1.000E+00
+ NF  = 1.000E+00 NCR = 1.000E+00 NCRP= 1.000E+00 NR  = 1.000E+00


MOD_PV693A01   728684734  96   200  100660 1355

**
**
* SIX 1.5 BY 45 MICRON STRIPES - NOM
**                                  JDJ/RDP 11/19/91
**
.MODEL PV693A01 USRMOD=PEB1 % PNP NOM  MODEL
+ RBX = 1.631E+00 RBI = 2.179E+00 RCX = 1.095E+01 RCI = 1.022E+01
+ RE  = 1.438E-01 IS  = 9.324E-16 I1  = 6.920E-18 I2  = 2.374E-14
+ NE  = 1.459E+00 IK  = 7.849E-02 VBO = 8.500E-01 TFO = 4.500E-12
+ CJE = 1.065E-12 PE  = 7.351E-01 ME  = 4.930E-01 BE  = 8.922E-02
+ I3  = 1.508E-17 I4  = 6.690E-15 NC  = 1.700E+00 IKR = 8.872E-01
+ VAO = 2.958E+00 TRO = 1.500E-10 CJC = 9.475E-14 PC  = 7.771E-01
+ MC  = 5.000E-01 BC  = 1.000E-01 EA  = 1.184E+00 DEA = 6.825E-02
+ TO  = 2.500E+01 KFN = 0.000E+00 AFN = 1.000E+00 BFN = 1.000E+00
+ BVBC= 0.000E+00 ALC1= 2.000E+00 ALC2= 0.000E+00 ALTC= 7.500E-01
+ BVBE= 0.000E+00 ALE1= 2.000E+00 ALE2= 0.000E+00 ALTE= 7.500E-01
+ NID = 2.932E-12 QCO = 7.615E-14 VJCO= 1.498E+00 TRCI= 2.000E+00
+ TVCO= 1.680E+00 RBIP= 7.474E+00 I1P = 3.867E-17 I2P = 1.023E-14
+ NEP = 1.722E+00 IKP = 8.004E-02 CJEP= 7.687E-13 ISP = 1.526E-17
+ I3P = 3.468E-16 CJCP= 2.530E-12 PS  = 9.082E-01 MS  = 4.931E-01
+ BS  = 1.000E-01 MTQB= 1.050E+00 DEA2= 1.778E-01 XTIS= 2.000E+00
+ XTI1= 3.000E+00 XTI2= 2.200E+00 QCOX= 3.808E-13 NFP = 1.000E+00
+ NF  = 1.000E+00 NCR = 1.000E+00 NCRP= 1.000E+00 NR  = 1.000E+00

**********************************************************************

!<arch>
SUB_RV80      682612593  96   200  100660 401
```

```
* LIBRARY UPDATE VERSION 1.2 8/19/91 10:37:24
* RESISTOR MODELS LIBRARY REVISED 8/26/87 BY WH ECKTON
* RESISTOR SUBCIRCUITS

SUB_RVL      682612594  96   200  100660  1201

* NEW MODELS AND NAMES RDP/TNT 8/16/91
* SUBCIRCUIT for 3 Terminal RES80 Resistor CBICV : NOMINAL
* RESISTOR has 4 nodes  RDP 5/3/90
* THIS MODEL CONTAINS THE FOLLOWING PARAMETERS:
*    DW   = CHANGE IN RESISTOR WIDTH (NOMINAL)
*    DWP  = CHANGE IN RESISTOR WIDTH DUE TO PROCESS VARIATION
*    WN   = NOMINAL RESISTOR WIDTH
*    WE   = EFFECTIVE RESISTOR WIDTH
*    WT   = WIDTH OF BASE P DIFFUSION (TO DETERMINE THE PARASITIC
CAPACITANCE)
*    DLP  = CHANGE IN RESISTOR WIDTH DUE TO PROCESS VARIATION,
NOT AVAILABLE
*    DLN  = CHANGE IN RESISTOR LENGTH (NOMINAL), DETERMINED
EXPERIMENTALLY
*    LT   = LENGTH OF RESISTOR TERMINAL
*    XJ   = JUNCTION DEPTH OF RES80

.SUBCIR RVL A B C {R=100,W=5,DW=-0.07,DWP=0.0,DLP=0.0}

 {XJ=0.26}
 {ARC=1.417*XJ}
 {RSN=80}
 {WN=W+DW}
 {WE=WN+DWP}
 {WT=WE+5}
 {DLN=1.033/(W+0.1)+0.034}
 {DL=DLN+DLP}
 {RTERM=RSN*DLN/WN}
 {LT=6.5}
 {L=(R-RTERM)*WN/RSN}
 R1 A D RVL00 {R/2*(WN/WE)*(L+DLP)/L}
 R2 D B RVL00 {R/2*(WN/WE)*(L+DLP)/L}
 DR#A A C DVR {WT*L/4+WT*LT+(L/2+2*LT+WT)*ARC}  OFF
 DR#B B C DVR {WT*L/4+WT*LT+(L/2+2*LT+WT)*ARC}  OFF
 DR#C D C DVR {WT*L/2+L*ARC} OFF

.FINIS

************************************************************************

* LIBRARY UPDATE VERSION 1.2 8/19/91 10:36:51
* RESISTOR MODELS LIBRARY REVISED 8/26/87 BY WH ECKTON
* RESISTOR SUBCIRCUIT
```

```
SUB_RVH      682612562  96   200   100660 1056

* NEW MODELS AND NAMES RDP/TNT 8/16/91
* SUBCIRCUIT for 3 Terminal PBASE Resistor CBICV : NOMINAL
* RESISTOR has 4 nodes  RDP 5/3/90
* THIS MODEL CONTAINS THE FOLLOWING PARAMETERS:
*     DW   = CHANGE IN RESISTOR WIDTH (NOMINAL)
*     DWP  = CHANGE IN RESISTOR WIDTH DUE TO PROCESS VARIATION
*     WN   = NOMINAL RESISTOR WIDTH
*     WTN  = NOMINAL RESISTOR TERMINAL WIDTH
*     WE   = EFFECTIVE RESISTOR WIDTH
*     DLP  = CHANGE IN RESISTOR LENGTH DUE TO PROCESS VARIATION
*          THIS IS THE SAME VALUE AS -DWP OF RVL
*
.SUBCIR RVH A B C {R=1K,W=10,DW=-0.1,DWP=-0.0,DLP=0.0}
 {XJH=0.16}
 {ARCH=1.417*XJH}
 {XJL=0.26}
 {ARCL=1.417*XJL}
 {RSN=1880}
 {WN=W+DW}
 {WE=WN+DWP}
 {WT=WE+3}
 {DLN=0.33-1.22/(W+0.1)}
 {RTERM=RSN*DLN/WN}
 {LT=9.5}
 {L=(R-RTERM)*WN/RSN}
 R1 A D RVH00 {R/2*(WN/WE)*(L+DLP)/L}
 R2 D B RVH00 {R/2*(WN/WE)*(L+DLP)/L}
 DR#A A C DVR {WE*L/4+WT*LT+L/2*ARCH+(2*LT+WT)*ARCL+WT*ARCL-
WE*ARCH}  OFF
 DR#B B C DVR {WE*L/4+WT*LT+L/2*ARCH+(2*LT+WT)*ARCL+WT*ARCL-
WE*ARCH}  OFF
 DR#C D C DVR {WE*L/2+L*ARCH} OFF
.FINIS

*********************************************************************


* ADVICE CAPACITOR MODELS
* NOMINAL PROCESSING
* NEW NAMES 9/6/91 SM
* NOTE THESE MODELS REFLECT CBIC-U PROCESSING
* THEY HAVE TO BE UPDATED FOR CBIC-V - SM 9/6/91

SUB_CVC      684425718  96   200   100660 216
* COMB CAPACITORS
.SUBCKT CVC (1, 2, 3) {C=10P,FRUSE=1.0,DVAR=1.0}
 {CP=C/FRUSE}
 C1 1 4 CVMNOS {C}
```

```
 RC#1 4 2 RVMNOS {13.2E-12/CP}
 DC#1 3 4 DE {DVAR*(0.46 + 1.088E+6*SQRT(CP))}
 DC#2 3 4 DS {6.11E12*CP}
.FINIS

* END OF MODELS
*******************************************************
```

APPENDIX B

Noise Analysis of Simple Differential Pair-

***** Noise at VOUT Frequency: 1.000E+04 hz Weight: 1.000E+00

Resistor contributions to output noise

Name	Total (sq v/hz)
R3	1.169E-52
R4	1.169E-52
XR1 .R1	4.071E-19
XR1 .R2	4.071E-19
XR2 .R1	4.071E-19
XR2 .R2	4.071E-19

Diode contributions to output noise

Name	RS	ID	FN	Total (sq v/hz)
XR1 .DR#A	0.000E+00	0.000E+00	0.000E+00	0.000E+00
XR1 .DR#B	2.751E-36	1.764E-28	0.000E+00	1.764E-28
XR1 .DR#C	1.401E-37	2.054E-29	0.000E+00	2.054E-29
XR2 .DR#A	0.000E+00	0.000E+00	0.000E+00	0.000E+00
XR2 .DR#B	2.751E-36	1.764E-28	0.000E+00	1.764E-28
XR2 .DR#C	1.401E-37	2.054E-29	0.000E+00	2.054E-29

User-Defined model contributions to output noise

name	RB	RC	RE	IB	IC	FN (sq v/hz)	PD	Total
B1	4.85E-18	6.86E-24	1.86E-19	1.89E-20	2.93E-18	0.00E+00	1.15E-28	7.99E-18

name	RB	RC	RE	IB	IC	FN (sq v/hz)	PD	Total
B2	4.85E-18	6.86E-24	1.86E-19	1.89E-20	2.93E-18	0.00E+00	1.15E-28	7.99E-18

Total output noise voltage = 1.760E-17 sq v/hz = 4.196E-09 v/rt hz

Total output noise power -1.675E+02 dbm/hz at 1 Kohm

Transfer function value (VOUT / VIN) 6.811E+00

Equivalent input noise (at VIN) 6.160E-10 v/rt hz

AC analysis completed
7 points to frequency: 1.000E+10

>>

APPENDIX C

Circuit Simulations-

***** Noise at VOUT Frequency: 1.000E+04 hz Weight: 1.000E+00

Input device noise contributions-

XUD_1LZ 1.25E-13 2.26E-19 4.78E-15 2.44E-15 8.47E-14 0.00E+00 1.08E-23
2.17E-13
.B1

name	RB	RC	RE	IB	IC	FN	PD	Total
						(sq v/hz)		

XUD_1LZ 4.16E-13 7.35E-19 1.59E-14 5.92E-16 2.68E-13 0.00E+00 6.43E-24
7.01E-13
.B1A

name	RB	RC	RE	IB	IC	FN	PD	Total
						(sq v/hz)		

XUD_1LZ 1.39E-13 2.51E-19 5.31E-15 2.28E-15 9.62E-14 0.00E+00 1.10E-23
2.43E-13
.B2

name	RB	RC	RE	IB	IC	FN	PD	Total
						(sq v/hz)		

XUD_1LZ 3.76E-13 6.66E-19 1.43E-14 4.12E-16 2.61E-13 0.00E+00 6.20E-24
6.52E-13
.B2A

name	RB	RC	RE	IB	IC	FN	PD	Total
						(sq v/hz)		

Summary of noise contributions from all components-

Total output noise voltage = 2.397E-12 sq v/hz = 1.548E-06 v/rt hz

Total output noise power -1.162E+02 dbm/hz at 1 Kohm

Transfer function value (VOUT / VDIFF) 1.942E+03

Equivalent input noise (at VDIFF) 7.972E-10 v/rt hz

AC analysis completed
7 points to frequency: 1.000E+10

Stability Analysis-

DC operating point analysis completed in 16 iterations

AC analysis completed
101 points to frequency: 1.000E+10

AC analysis completed
101 points to frequency: 1.000E+10

Phase margin = 55.25 degrees at frequency = 3.098E+08

Gain margin = 4.92 db at frequency = 6.946E+08

>>

Total Harmonic Distortion Analysis-

****
*

* External Setup for THD- "thd_setup" - ADVICE -

Fourier analysis Temperature 25.000 Deg C

****
*

***** Fourier components of transient response VOUT

dc component = -3.028E-03

harmonic no	frequency (hz)	Fourier component	normalized component	phase (deg)	normalized phase (deg)
1	1.000E+06	1.999E+00	1.000000	-0.173	0.000
2	2.000E+06	5.559E-05	0.000028	88.001	88.174
3	3.000E+06	7.584E-05	0.000038	-82.156	-81.983
4	4.000E+06	1.752E-06	0.000001	-59.887	-59.714
5	5.000E+06	5.704E-05	0.000029	-93.851	-93.678
6	6.000E+06	2.584E-06	0.000001	96.141	96.314
7	7.000E+06	3.783E-05	0.000019	-92.115	-91.942
8	8.000E+06	1.992E-06	0.000001	98.983	99.156
9	9.000E+06	2.676E-05	0.000013	-92.693	-92.520

total harmonic distortion = 0.006 %

>>

APPENDIX D

AT&T'S CBIC-V TECHNOLOGY

The performance of many linear circuits fabricated in a typical analog bipolar process is often limited by the lack of PNP transistors having similar gain and frequency characteristics of NPN transistors. Several manufacturers have addressed this problem by developing complementary bipolar processes based on either junction-isolated or dielectric-isolated technologies. Complementary devices are particularly useful in applications requiring good power supply and common-mode rejection, low noise performance, low input capacitance, low power, and high gain-bandwidth products.

CBIC-V, a development of AT&T Bell Laboratories and AT&T Microelectronics, is a complementary bipolar integrated circuit technology offering vertical NPN transistors having a nominal peak ft value of 11.2 GHz and vertical PNP transistors having a nominal peak ft value of 5.6 GHz. Besides transistors, the CBIC technology supports a variety of resistor and capacitor structures. Interconnect is accomplished using two levels of gold metallization, each having the same low sheet resistance of 0.04 ohms/sq. and a trace width current-carrying capability of 2 mA/um.

The high level of performance achieved by the CBIC process depends heavily upon advantages gained through use of a novel fabrication technique known as Selective Epitaxial Growth (SEG). SEG is used to achieve compact, planar isolation between components. N and p-type epitaxial films are grown on heavily doped arsenic and boron buried layers. Because high speed requirements translate into shallow junction depths, reduced temperature processing techniques including low energy ion implantation, rapid

thermal anneal (RTA) and low temperature dielectrics are employed instead of more conventional processing methods.

The transistor design uses a conventional vertical structure which reflects the need for a robust, high-yield process which is compatible with existing equipment capabilities. Cross-sectional views of both NPN and PNP devices are shown in Figures 26 and 27, respectively. The NPN transistor contains features necessary for high speed and low noise devices, including a buried layer, deep collector contacts, and striped bases and emitters. The NPN device also has a channel-stop layer to prevent surface inversion of the lightly doped p-type substrate. The PNP transistor shown in Figure 27 has all of the features of the NPN device except the channel stop, but is of opposite type conductivity. The PNP device also employs a lightly doped n-type region for collector isolation and a buried n-type region for collector isolation from the p-substrate. In operation, a reverse bias is applied to the buried n-layer to reduce the collector-substrate parasitic capacitance.

A variety of different-size devices are constructed using the same basic physical structure just described. AT&T defines the smallest device available in CBIC-V as having one emitter stripe 5 um long and one collector contact (NV111A01 or PV111A01). AT&T names its devices using the following scheme:

N - Type of device (N=NPN, P=PNP)

V - Technology (CBIC-V)

2 - Number of emitter stripes per device

3 - Length of each emitter stripe
divided by 5 um (ex: 3 ==> 15 um)

1 - Number of collector contacts

A - Version (A)

0 - Layout style (0 for standard device)

1 - Number of devices within same isolation

A scaling factor may also follow the transistor name (for example, "NV231A01 3" indicates three NV231A01 devices connected in parallel.) Integers greater than 9 are represented by alpha characters (for example, A=10, B=11, C=12, etc.) The maximum emitter stripe length is 50 um.

Figure 28 lists electrical characteristics for both the NV231A01 and PV231A01 devices. These devices have two emitter stripes which are each 15 um long by 1.5 um wide. These attributes can be used to estimate the electrical characteristics for different size devices provided that the stated currents are scaled appropriately.

Care must be taken in the design process to ensure that the stated breakdown voltages are not exceeded. Because of the shallow junction depths dictated by high speed requirements, a basic tradeoff exists between speed and breakdown voltage. Both the NPN and PNP devices list a 6 V minimum value for BVCEX. An updated process called CBIC-V2 guarantees an 8 V minimum value for BVCEX. This suggests that in order to design a manufacturable circuit that does not violate the stated breakdown criteria, collector to emitter voltage must not exceed 8 V in magnitude. The breakdown mechanisms responsible include both avalanche or carrier multiplication and punch-thru or base depletion.

Useful plots of typical device characteristics are presented in Figures 29 through 34. These graphs include frequency response, current gain, output voltage, collector

current vs. saturation voltage, collector current vs. base-emitter voltage, and collector breakdown characteristics.

Selection of transistor size is typically based on many factors including requirements for current handling, device pair matching, parasitic capacitance and layout considerations. The lookup tables shown in Figures 35 and 36 are helpful in device size selection. For each device, listed characteristics include an emitter area scale factor, ranges of current where the device operates within 80% of its peak beta and 80% of its peak ft, the maximum recommended dc current, nominal zero bias capacitances, and the device size.

Besides transistors, CBIC-V offers a variety of resistor structures including two types of diffused resistors. One type has a sheet resistance of 80 ohms/square (called RVL) while the other type has a sheet resistance of 1880 ohms/square (called RVH). A cross section of the resistor structure and its subcircuit model are shown in Figure 37. The diffused resistors in CBIC-V consist of a p type region sitting in an n type epitaxial tub. By reverse biasing this pn junction, electrical isolation can be achieved. Designers must keep in mind the potential effects of parasitic capacitance due to this junction. For this reason, the simulation models include parasitic diodes to represent these junctions. In addition to diffused resistors, high-precision thin-film tantalum-nitride resistors are offered as an option to the normal process. Figure 38 summarizes the characteristics of the three types of resistors available. A fusible link trim capability is also available to adjust circuit parameters during testing by adding more resistance to a path.

CBIC-V supports two types of capacitor structures: Metal-Nitride-Oxide-Silicon (MNOS) and Metal-On-Metal (MOM). MNOS capacitors are used for capacitance

values greater than 0.55 pF while MOM capacitors are used for smaller values. The MNOS capacitor structure and its subcircuit model are shown in Figure 39. Isolation is provided by forcing the substrate to the most negative potential of the circuit, thereby always reverse-biasing the diodes shown in the model. The MOM capacitor is formed simply by using top and bottom metal, as shown in Figure 40. Capacitor characteristics are presented in Figure 41.

The types of devices just described are typically laid out in a customized fashion to minimize total chip area and layout parasitics. A custom layout and fabrication process demands a great deal of time and money. A more cost effective and timely approach involves the use of what is called a "linear array", where a predesigned template of devices are laid out and fabricated, needing only a custom metallization pattern to complete processing. Although layout parasitics will be higher compared to a custom layout, circuit performance often approaches that of a full custom layout. The designer can customize the bottom-metal, via holes, top-metal, and thin film resistor levels. Figure 42 summarizes the type and number of components available on the AT&T ALA110 VHF Semi-Custom Linear Array.

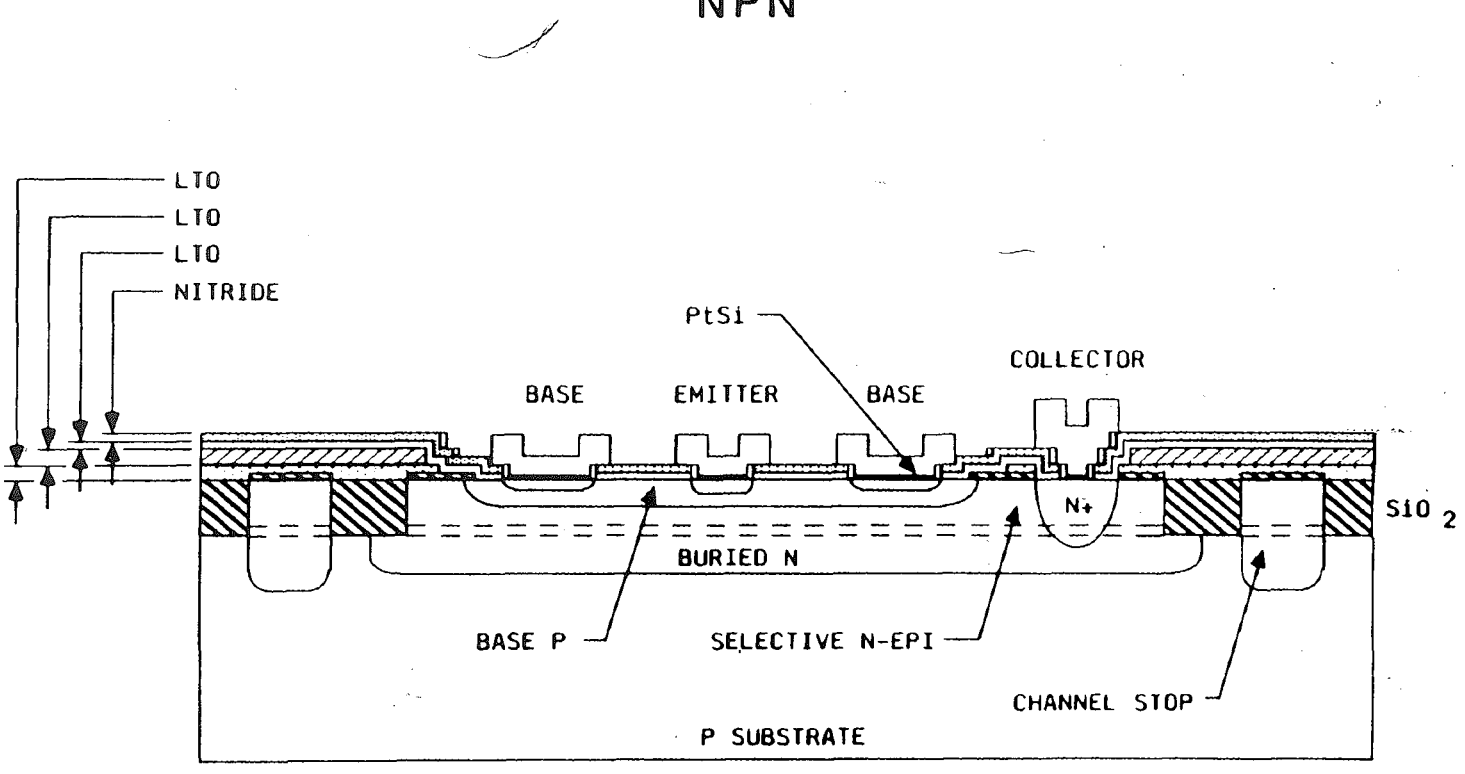


Figure 26. Cross Sectional View of NPN Transistor

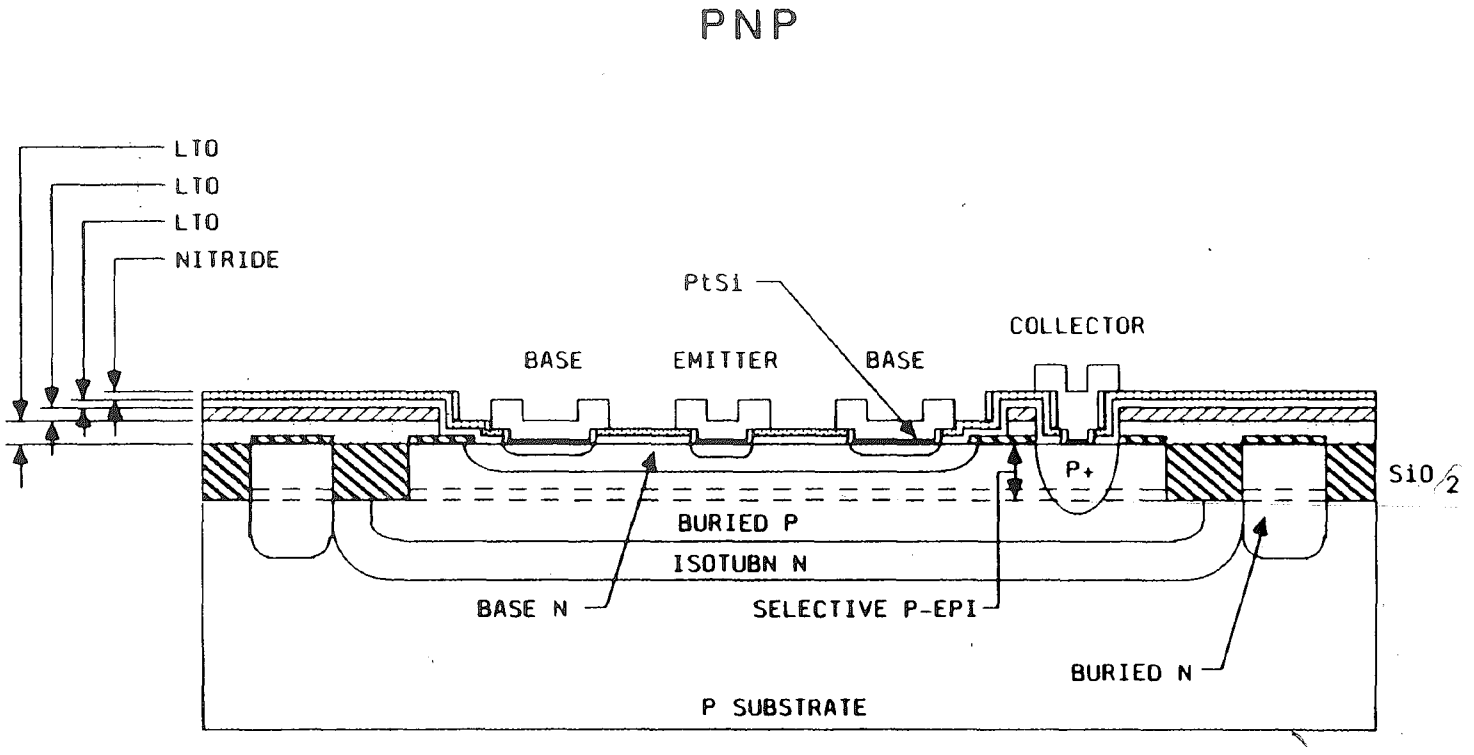


Figure 27. Cross Sectional View of PNP Transistor

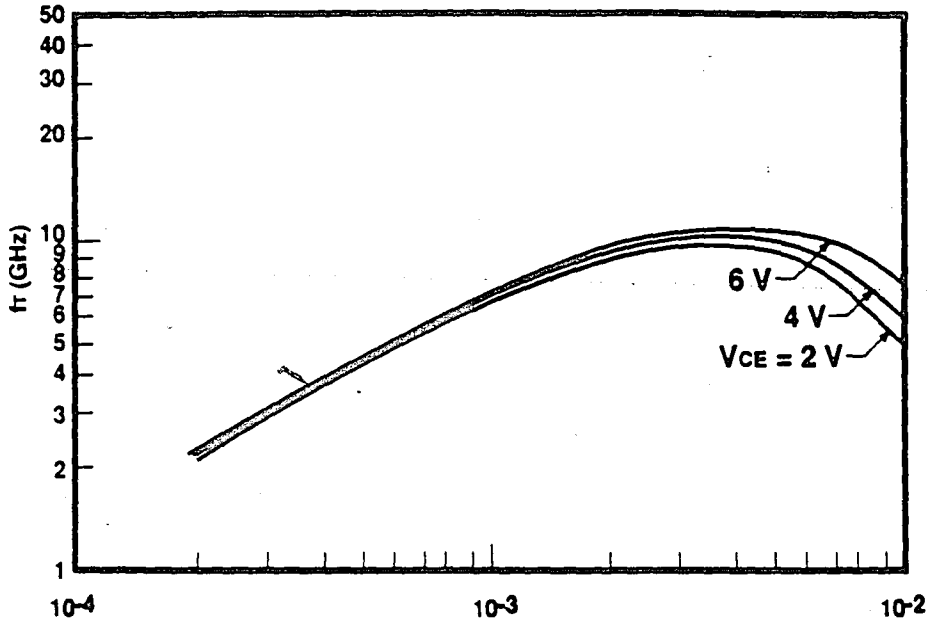
TABLE 2. NPN (NV231A01) Characteristics (TA = 25°C)

Parameter	Measurement Condition	Limits			Units
		Min	Typ	Max	
HFE	IC = 1 mA, VCB = 2 V	50	118	–	–
fT	IC = 4 mA, VCE = 3 V	8	10.2	–	GHz
VA	IC = 1 mA, VCE = 2, 4 V	12	27	–	V
VCE(sat)	IC = 1 mA, IB = 100 µA	–	86	180	mV
VBE	IE = –1 mA, VCB = 2 V	740	780	810	mV
BVCEX	IC = 100 µA, IB = 0.1 µA	6	11.5	–	V
BVCBO	IC = 1 µA	6	19	–	V
BVCIO	IC = 1 µA	25	45	–	V
BVEBO	IE = 10 µA	2	–	–	V
BVEBS	IE = 1 µA	0.2 *	–	–	V

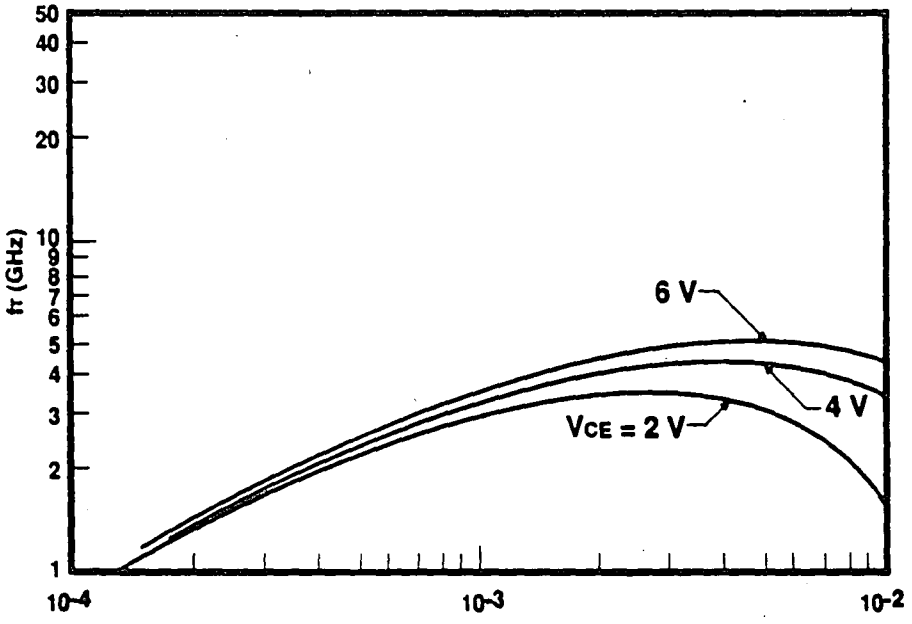
PNP (PV231A01) Characteristics (TA = 25°C)

Parameter	Measurement Condition	Limits			Units
		Min	Typ	Max	
HFE	IC = –1 mA, VCB = –2 V	25	45	–	–
fT	IC = –3 mA, VCE = –3 V	3	4.3	–	GHz
VA	IC = –1 mA, VCE = –2, –4 V	6	11	–	V
VCE(sat)	IC = –1 mA, IB = –100 µA	–	–188	–360	mV
VBE	IE = 1 mA, VCB = –2 V	–750	–792	–830	mV
BVCEX	IC = –100 µA, IB = –0.1 µA	6	15	–	V
BVCBO	IC = –1 µA	8	22	–	V
BVCIO	IC = –1 µA	11	17	–	V
BVEBO	IE = –10 µA	–3.5	–	–	V
BVEBS	IE = –1 µA	0.1 *	–	–	V

Figure 28. List of Electrical Characteristics For NV231A01 And PV231A01 Devices

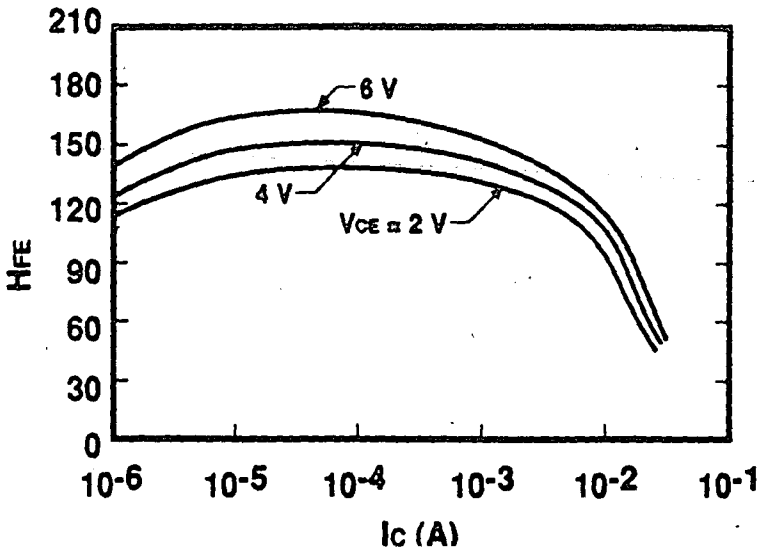


Typical Unity Gain Frequency Response (NV231A01)

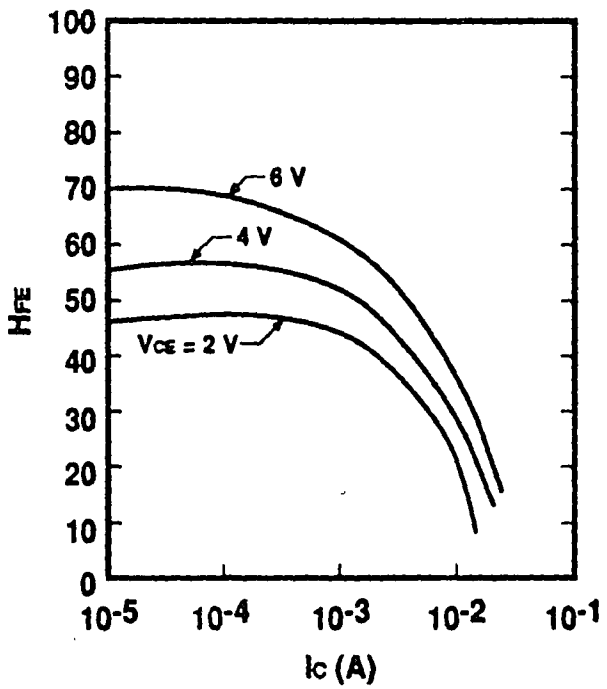


Typical Unity Gain Frequency Response (PV231A01)

Figure 29. Transistor Unity Gain Frequency Response Plots

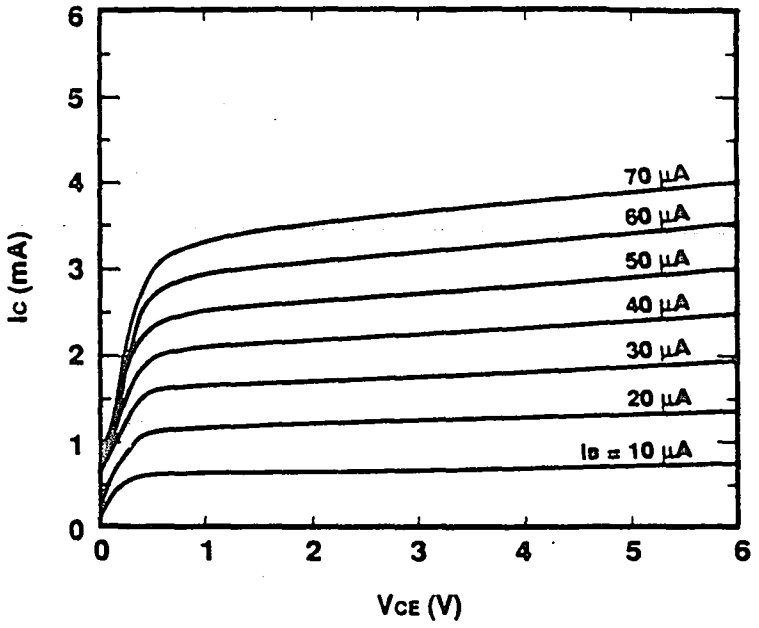


Typical Current Gain Characteristics (NV231A01)

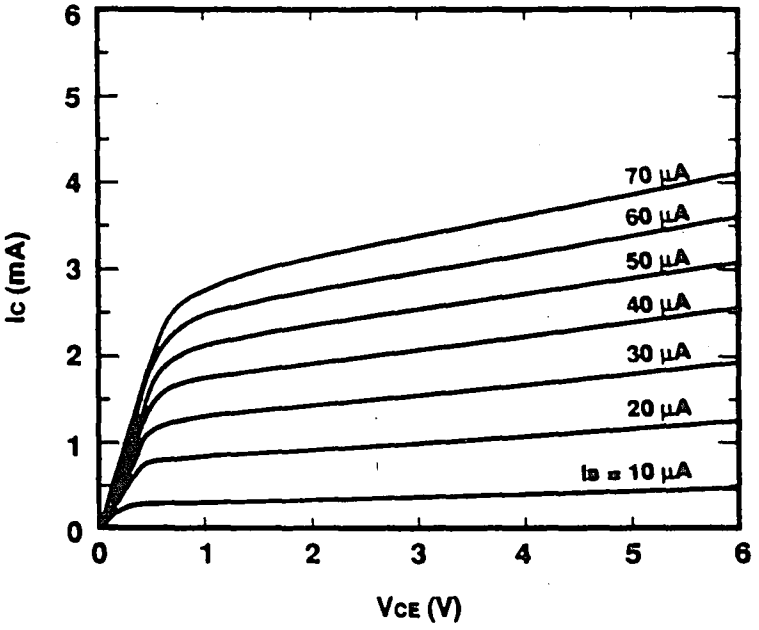


Typical Current Gain Characteristics (PV231A01)

Figure 30. Typical Transistor Current Gain Characteristics

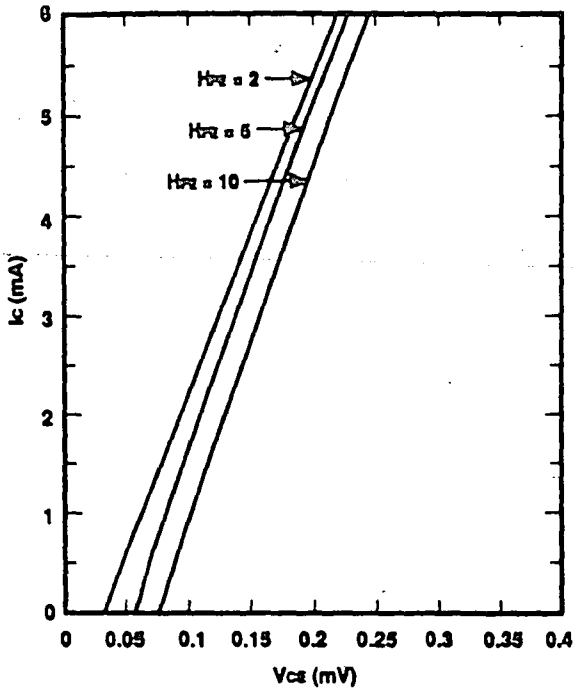


Typical Output Voltage Characteristics (NV231A01)

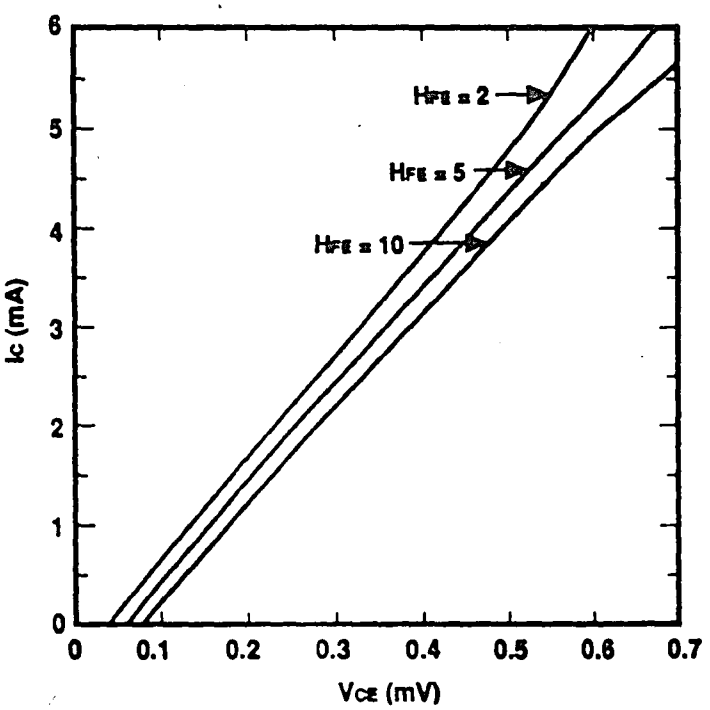


Typical Output Voltage Characteristics (PV231A01)

Figure 31. Typical Transistor Output Voltage Characteristics

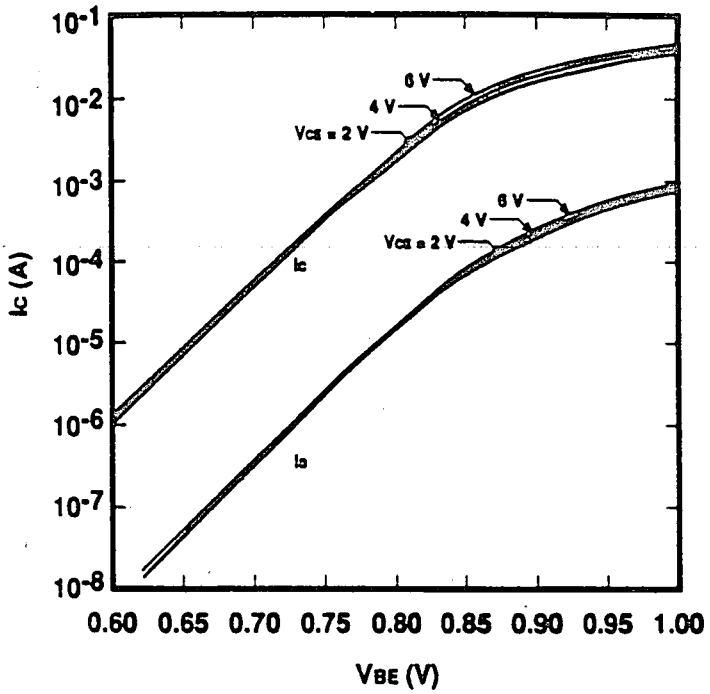


Typical Current vs. Saturation Voltage (NV231A01)

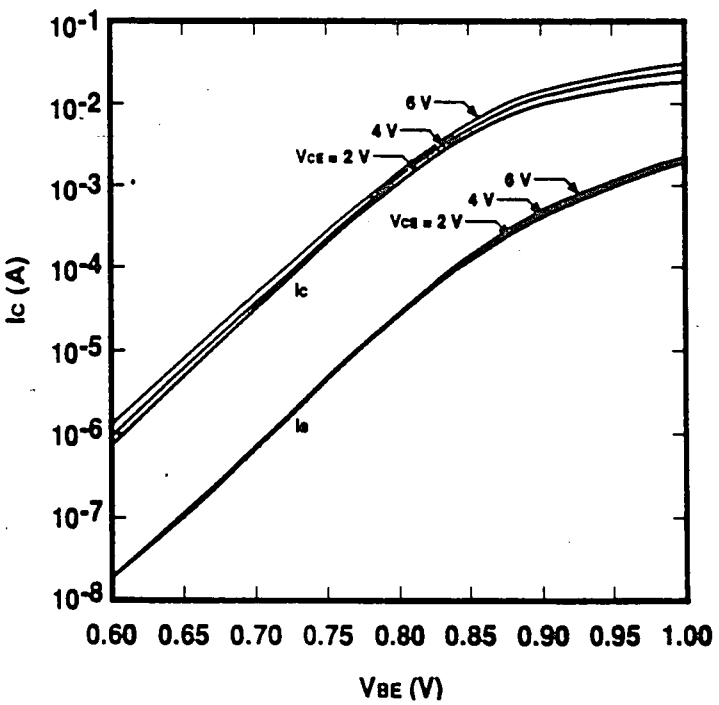


Typical Current vs. Saturation Voltage (PV231A01)

Figure 32. Typical Transistor Collector Current Versus Saturation Voltage

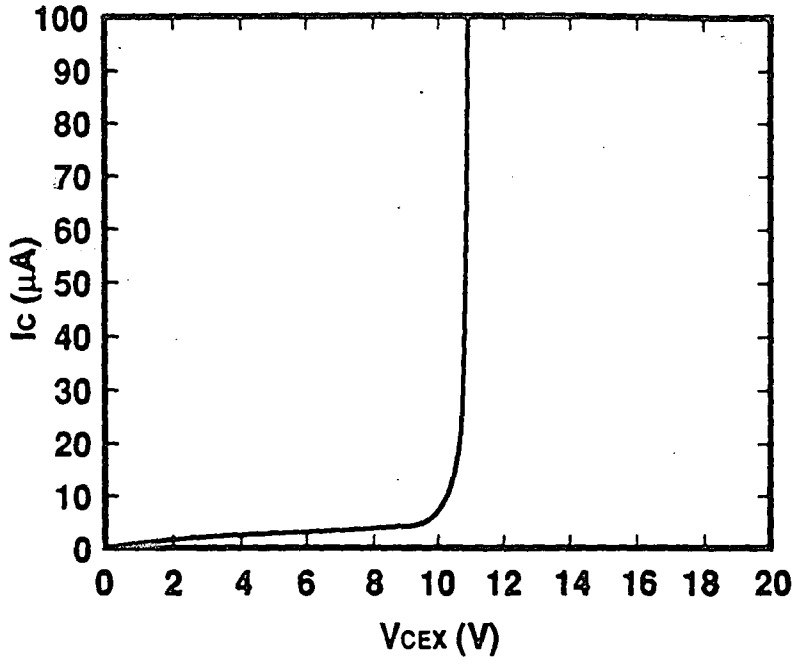


Typical Current vs. Voltage Characteristics (NV231A01)

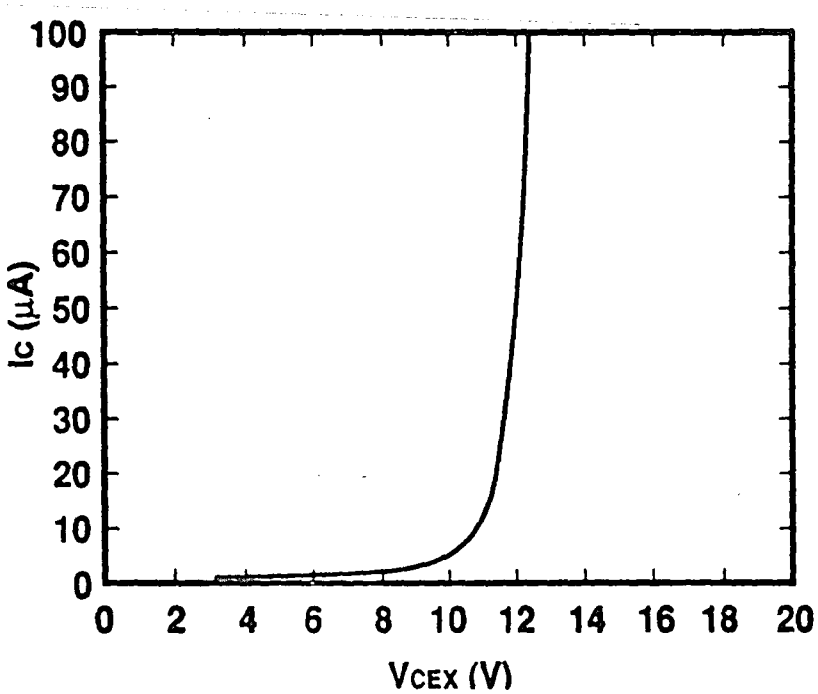


Typical Current vs. Voltage Characteristics (PV231A01)

Figure 33. Typical Transistor Collector Current Versus Base-To-Emitter Voltage



Typical Collector Breakdown Characteristics (NV231A01)



Typical Collector Breakdown Characteristics (PV231A01)

Figure 34. Typical Transistor Collector Breakdown Characteristics

CBIC-V Standard NPN Transistors for Custom Circuits

Name	Scale	Current Range 80% Beta (mA)		Current Range 80% fT (mA)		Max. dc	CJE VBE = 0	CJC VBC = 0	CJS VCS = 0	Size (μm x μm)
		Min	Max	Min	Max	I (mA)	pF	pF	pF	
NV111A01	1	0.01	0.3	0.3	1.2	1.2	0.02	0.02	0.05	22.5 x 37.5
NV121A01	2	0.02	0.7	0.6	2.5	2.4	0.04	0.04	0.06	27.5 x 37.5
NV221A01	4	0.03	1.3	1.2	5.0	4.8	0.08	0.06	0.08	27.5 x 47.5
NV321A01	6	0.05	2.0	1.8	7.5	7.2	0.12	0.08	0.10	27.5 x 57.5
NV422A01	8	0.07	2.7	2.4	10.0	9.6	0.16	0.10	0.14	40.0 x 75.0
NV131A01	3	0.03	1.0	0.9	3.8	3.6	0.06	0.05	0.08	32.5 x 37.5
NV231A01	6	0.05	2.0	1.8	7.5	7.2	0.12	0.08	0.10	32.5 x 47.5
NV331A01	9	0.08	3.0	2.7	11.2	10.8	0.18	0.11	0.13	32.5 x 57.5
NV431A01	12	0.10	4.0	3.6	15.0	14.4	0.24	0.14	0.15	32.5 x 67.5
NV141A01	4	0.03	1.3	1.2	5.0	4.8	0.08	0.06	0.09	37.5 x 37.5
NV241A01	8	0.07	2.7	2.4	10.0	9.6	0.16	0.10	0.12	37.5 x 47.5
NV341A01	12	0.10	4.0	3.6	15.0	14.4	0.24	0.13	0.15	37.5 x 57.5
NV442A01	16	0.13	5.3	4.8	20.0	19.2	0.32	0.17	0.20	37.5 x 75.0
NV151A01	5	0.04	1.6	1.5	6.3	5.0*	0.10	0.07	0.11	42.5 x 37.5
NV251A01	10	0.08	3.3	3.0	12.5	10.0*	0.20	0.12	0.14	42.5 x 47.5
NV351A01	15	0.12	5.0	4.5	18.8	15.0*	0.30	0.16	0.17	42.5 x 57.5
NV452A01	20	0.17	6.7	6.0	25.0	20.0*	0.40	0.21	0.22	42.5 x 75.0
NV652A01	30	0.25	10.0	9.0	37.5	30.0*	0.59	0.29	0.29	42.5 x 95.0
NV362A01	18	0.15	6.0	5.4	22.5	15.0*	0.36	0.19	0.22	27.5 x 65.0
NV462A01	24	0.20	8.0	7.2	30.0	20.0*	0.47	0.24	0.25	47.5 x 75.0
NV663A01	36	0.30	12.0	10.8	45.0	30.0*	0.71	0.38	0.39	47.5 x 132.5
NV863A01	48	0.40	16.0	14.4	60.0	40.0*	0.95	0.48	0.46	47.5 x 152.5
NV472A01	28	0.23	9.3	8.4	35.0	20.0*	0.55	0.27	0.28	52.5 x 75.0
NV673A01	42	0.35	14.0	12.6	52.5	30.0*	0.83	0.43	0.43	65.0 x 115.0
NV883A01	64	0.53	21.3	19.2	80.0	40.0*	1.26	0.62	0.56	70.0 x 135.0
NV392A01	27	0.23	9.0	8.1	33.8	15.0*	0.53	0.27	0.29	75.0 x 65.0
NV693A01	54	0.45	18.0	16.2	67.5	30.0*	1.06	0.54	0.52	70.0 x 115.0
NV893A01	72	0.60	24.0	21.6	90.0	40.0*	1.42	0.69	0.61	75.0 x 135.0

* Maximum current limited by metallization at 5 mA/stripe.

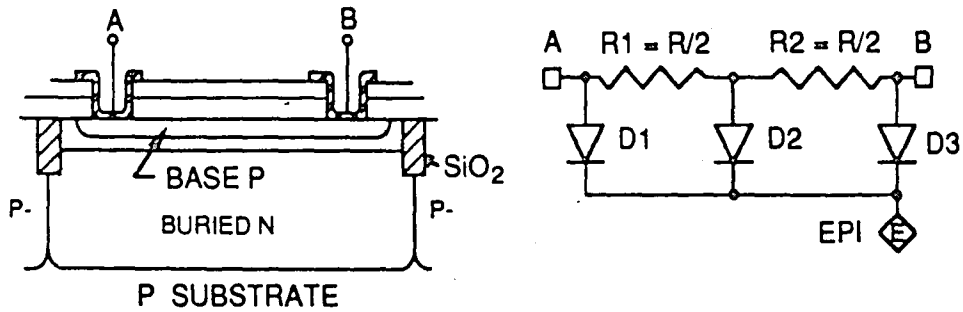
Figure 35. CBIC-V NPN Transistor Characteristics

CBIC-V Standard PNP Transistors for Custom Circuits

Name	Scale	Current Range 80% Beta (mA)		Current Range 80% ft (mA)		Max. dc	CJE VBE = 0	CJC VBC = 0	CJS VCS = 0	Size (μm x μm)
		Min	Max	Min	Max	I (mA)	pF	pF	pF	
PV111A01	1	0.01	0.3	0.2	0.7	1.2	0.02	0.04	0.26	22.5 x 37.5
PV121A01	2	0.01	0.7	0.4	1.4	2.4	0.04	0.06	0.33	27.5 x 37.5
PV221A01	4	0.02	1.3	0.7	2.8	4.8	0.06	0.09	0.42	27.5 x 47.5
PV321A01	6	0.04	2.0	1.1	4.2	7.2	0.12	0.13	0.52	27.5 x 57.5
PV422A01	8	0.05	2.7	1.5	5.7	9.6	0.16	0.17	0.69	27.5 x 75.0
PV131A01	3	0.02	1.0	0.6	2.1	3.6	0.06	0.08	0.39	32.5 x 37.5
PV231A01	6	0.04	2.0	1.1	4.2	7.2	0.12	0.13	0.51	32.5 x 47.5
PV332A01	9	0.06	3.0	1.6	6.4	10.8	0.18	0.17	0.71	32.5 x 65.0
PV432A01	12	0.07	4.0	2.2	8.5	14.4	0.24	0.22	0.83	32.5 x 75.0
PV141A01	4	0.02	1.3	0.7	2.8	4.8	0.08	0.10	0.46	37.5 x 37.5
PV241A01	8	0.05	2.7	1.5	5.7	9.6	0.16	0.16	0.59	37.5 x 47.5
PV342A01	12	0.07	4.0	2.2	8.5	14.4	0.24	0.22	0.83	37.5 x 65.0
PV442A01	16	0.10	5.3	2.9	11.3	19.2	0.32	0.28	0.97	37.5 x 75.0
PV151A01	5	0.03	1.7	0.9	3.6	5.0*	0.10	0.12	0.53	55.0 x 37.5
PV251A01	10	0.06	3.3	1.8	7.1	10.0*	0.20	0.19	0.68	42.5 x 47.5
PV352A01	15	0.09	5.0	2.8	10.6	15.0*	0.30	0.26	0.95	42.5 x 65.0
PV452A01	20	0.12	6.7	3.7	14.2	20.0*	0.40	0.33	1.11	42.5 x 75.0
PV652A01	30	0.18	10.1	5.6	21.3	30.0*	0.59	0.47	1.41	55.0 x 95.0
PV362A01	18	0.11	6.0	3.3	12.8	15.0*	0.36	0.30	1.07	47.5 x 65.0
PV462A01	24	0.15	8.0	4.4	17.0	20.0*	0.47	0.38	1.25	47.5 x 75.0
PV663A01	36	0.22	12.0	6.6	25.5	30.0*	0.71	0.60	1.90	60.0 x 115.0
PV863A01	48	0.29	16.1	8.9	34.1	40.0*	0.95	0.77	2.24	52.0 x 152.5
PV472A01	28	0.17	9.4	5.2	19.9	20.0*	0.55	0.44	1.38	65.0 x 77.5
PV673A01	42	0.25	14.1	7.8	29.8	30.0*	0.83	0.69	2.11	65.0 x 115.0
PV883A01	64	0.38	21.4	11.8	45.4	40.0*	1.26	0.99	2.74	57.5 x 152.5
PV392A01	27	0.16	9.1	5.0	19.2	15.0*	0.53	0.43	1.43	75.0 x 67.5
PV693A01	54	0.33	18.0	9.9	38.2	30.0*	1.06	0.86	2.53	62.5 x 132.5
PV893A01	72	0.44	24.0	13.2	51.0	40.0*	1.42	1.10	2.99	62.5 x 152.5

* Maximum current limited by metallization at 5 mA/stripe.

Figure 36. CBIC-V PNP Transistor Characteristics



Resistor Structure and Subcircuit Model

Figure 37. Resistor Structure And Subcircuit Model

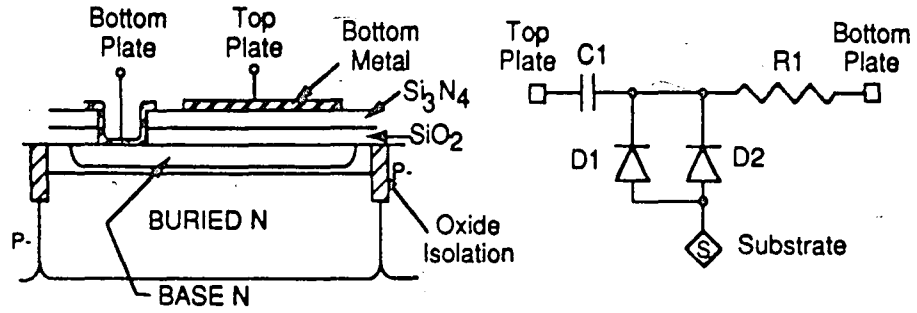
Resistor Characteristics (TA = 25°C)

Parameter		Resistor Types			Units
		RVL	RVH	STIC	
Sheet Resistance		80	1880	300	Ω/sq
Mismatch		±1*	±1*	±1.5**	%
Voltage Coeff.		negligible	0.4	negligible	%/V
1st Temp. Coeff., TC1		1.34E – 03	1.769E – 03	–200E – 06	$°C^{-1}$
2nd Temp. Coeff., TC2		1.0E – 06	5.638E – 06	negligible	$°C^{-2}$
Minimum Width		5	5	10	µm
Recommended	5 µm	95	1980	–	Ω
Minimum Value	10 µm	60	1225	–	Ω

* For similar size resistors located near each other.

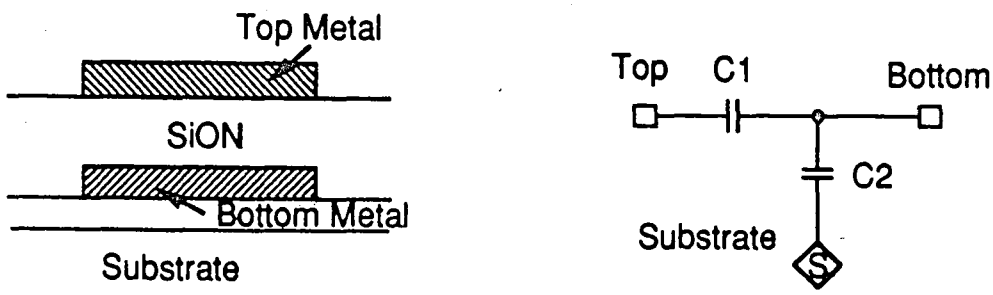
** For untrimmed resistors of similar size located near each other.

Figure 38. Resistor Characteristics



MNOS Capacitor Structure and Subcircuit Model

Figure 39. MNOS Capacitor Structure And Subcircuit Model



MOM Capacitor Structure and Subcircuit Model

Figure 40. MOM Capacitor Structure And Subcircuit Model

Capacitor Characteristics (TA = 25°C)

Parameter	Capacitor Types		Units
	MNOS	MOM	
Capacitance Density	2.22E-4	4.4E-5	pF/(μm^2)
Area/pF	4503	22660	(μm^2)/pF
Absolute Tolerance	±25	±35	%
Minimum Value	0.55	0.005	pF

Figure 41. Capacitor Characteristics

The following is a summary of the type and number of components available on the ALA110 VHF Semi-Custom Linear Array:

Transistors

NPN			PNP		
NV231A01	(6X)	- 27	PV231A01	(6X)	- 22
NV431A01	(12X)	- 20	PV432A01	(12X)	- 15
NV362A01	(18X)	- 2	PV392A01	(27X)	- 2
NV663A01	(36X)	- 2	PV693A01	(54X)	- 2

Resistors

80 Ω/sq.	1880 Ω/sq.
25 Ω - 16	2,000 Ω - 64
50 Ω - 2	10,000 Ω - 10
200 Ω - 154	Trimmable *
500 Ω - 16	

MNOS Capacitors

1.0 pF - 2
2.0 pF - 2
3.0 pF - 2
6.0 pF - 4
10.0 pF - 4

* 0.56 mm^2 is provided for thin-film (STIC) resistors.

Figure 42. Summary of Components Available On The ALA110 Linear Array

VITA

John Young Fizette received a B.S. degree in electrical engineering in 1987 and an M.S. degree in electrical engineering in 1993, both from Lehigh University. He was born January 12, 1965 in the city of East Stroudsburg, PA to William B. and Marjorie Y. Fizette.

Since 1988, he has worked for AT&T Microelectronics in Reading, PA, as a bipolar integrated circuit test engineer. His primary job function involves working with OEM customers to develop testing for high speed analog application specific integrated circuits. He is currently a test engineer in the Wireless Development Organization. Mr. Fizette is also a captain in the Air Force Reserve working in the field of aircraft maintenance.

END

OF

TITLE